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Device characteristics of InSnO thin-film transistors with a modulated channel

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Abstract
The device performance of channel-modulated InSnO thin-film transistors (TFTs) was investigated. The field-effect mobility in the channel-modulated TFTs with a high carrier concentration layer at the channel/gate insulator interface was enhanced due to the increased carrier concentration. The insertion of the high carrier concentration layer at the channel/electrode interface improved the device performance due to reduction of the parasitic resistance. These results indicated that the device characteristic of TFTs can be enhanced by the modulated channel structure.

(Some figures may appear in colour only in the online journal)

1. Introduction

Oxide semiconductor materials such as In_2O_3, In_2O_3-ZnO (IZO) and In_2O_3-SnO_2 (ITO) have been investigated for use in thin-film transistors (TFTs) since they can simultaneously be applied as a channel layer and electrode [1–3]. The field-effect mobility (μ_{FE}) and threshold voltage (V_{th}) are important parameters of TFTs, and it is difficult to acquire a high μ_{FE} and suitable V_{th} because they depend on the carrier concentration in the channel layer. Many researchers have focused on the dielectric layer, channel structure and the interface between the channel and electrode in order to improve the performance of oxide-based TFTs [4–13]. The device performance of TFTs has been enhanced due to the reduced interface traps by the bilayer dielectrics and well-defined interface [4, 5]. By inserting a layer with high carrier concentration between the channel and electrode, the performance of TFTs was enhanced due to the decreased parasitic contact resistance [6–8]. Ar plasma treatment at the interface of the channel and electrode results in an improvement of the performance of TFTs by reducing the parasitic contact resistance [9]. However, additional processes should be applied in these methods. TFTs with a double-channel layer have demonstrated the enhanced device performances by using a sublayer with high carrier concentration at the interface of the channel and gate oxide [10–13]. However, there have been no reports on how the modulated channel structure affects the performance of TFTs. In this study, channel-modulated TFTs were fabricated, and the device characteristics were characterized. In order to improve the performance of the TFTs, a new channel structure was suggested to combine the advantage of the double-channel layer and the insertion of a high carrier concentration layer between the channel and electrode.

2. Experimental details

The TFTs were fabricated on 300 nm thick SiO_2/heavily doped p-type Si substrates. 25 nm thick ITO channel layers were deposited by dc magnetron sputtering at a power of 80 W at room temperature. The flow rate of Ar was fixed at 20 sccm, and the O_2 flow rate was varied from 3.5 to 4.5 sccm. Al was deposited for the source and drain electrodes by thermal evaporation through a shadow mask. The channel length and width of the tested TFTs were 100 and 1000 μm, respectively. The thickness of the channel layer was measured using an ellipsometer (Rudolph Auto EL II). X-ray photoelectron spectroscopy (XPS) was also performed using Al twin anode x-ray sources (Al Kα line = 1486.6 eV). The electrical characteristics of the TFTs were measured using a Keithley 236 source measure unit.

3. Results and discussion

Figure 1 shows the channel structure of ITO TFTs, where channels 1 and 2 indicate a high carrier concentration layer and

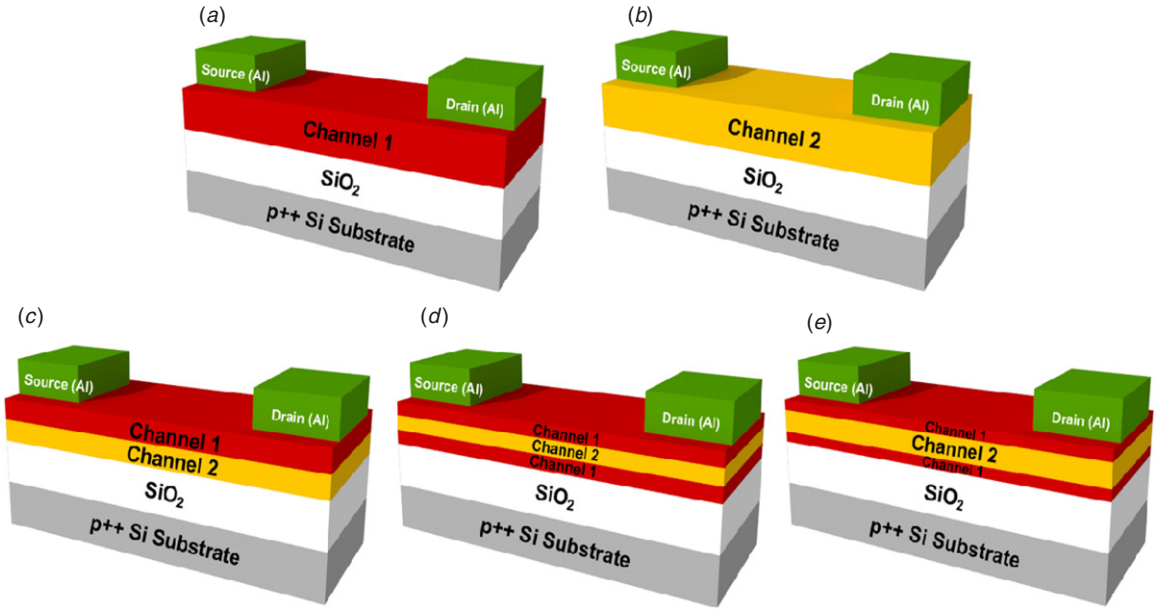

Figure 1. The structure of TFTs with (*a*) a one-channel layer with high carrier concentration, (*b*) a one-channel layer with low carrier concentration, (*c*) double-channel layers with low and high carrier concentration and (*d*, *e*) multiple-channel layers with high, low and high carrier concentrations with thickness variation.

a low carrier concentration layer, respectively. Figures 1(*a*) and (*b*) show the one-channel TFTs. Figure 1(*c*) shows the double-channel TFT and figures 1(*d*) and (*e*) show the multiple-channel TFTs with thickness variation. The detailed information of the TFT fabrication process is described below. The charge density of the ITO channel is calculated by using the equation [14]

$$N_{\mathrm{ch}} = C_i V_{\mathrm{on}} / q t_c \tag{1}$$

where C_i, V_{on}, q and t_c are the gate dielectric capacitance per unit area, turn-on voltage, elementary charge and channel thickness, respectively. From the equation, the charge density values of channels 1 and 2 were -5.18×10^{17} and $+1.08 \times 10^{17}$ cm^{-3}, respectively.

Figure 2(*a*) shows the transfer characteristics of the ITO TFTs at various O_2 flow rates. At an O_2 flow rate of 3.5 sccm, it is difficult to turn down the TFT due to the high electron concentration in the channel. As the O_2 flow rate increased from 3.5 to 4 sccm (TFT 1), the threshold voltage (V_{th}) became -13.1 V from the transfer characteristics appearing in figure 2(*a*). The field-effect mobility (μ_{FE}), subthreshold swing (S_{SUB}) and on/off current ratio ($I_{\mathrm{on/off}}$) were 19.0 cm^2 V^{-1} s^{-1}, 1.06 V dec^{-1}, and 3.4×10^7, respectively. When the O_2 flow rate increased to 4.5 sccm (TFT 2), V_{th} was positively shifted to 6.5 V and the on-state current decreased. μ_{FE}, S_{SUB} and $I_{\mathrm{on/off}}$ were reduced to 4.5 cm^2 V^{-1} s^{-1}, 0.77 V dec^{-1} and 1.9×10^6, respectively. Since the electron concentration in the oxide channel layer originated from oxygen vacancies [15], the increase of the O_2 flow rate suppressed the electron concentration in the channel layer and positively shifted V_{th}. μ_{FE} was reduced due to the decreased electron concentration in the channel and S_{SUB} was enhanced due to the decreased density of interface trap states between the channel and the dielectric layer [16]. Figure 2(*b*) shows the total resistance (R_{T})

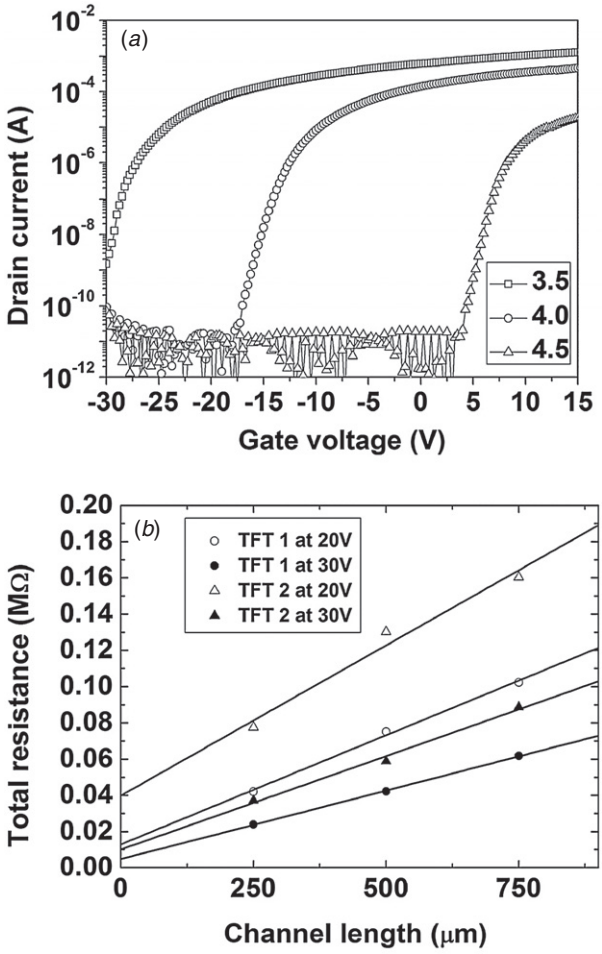

Figure 2. (*a*) The transfer characteristics of the ITO TFTs at various O_2 flow rates and (*b*) the total resistance versus channel length plots of TFTs 1 and 2 at gate voltages of 20 and 30 V.

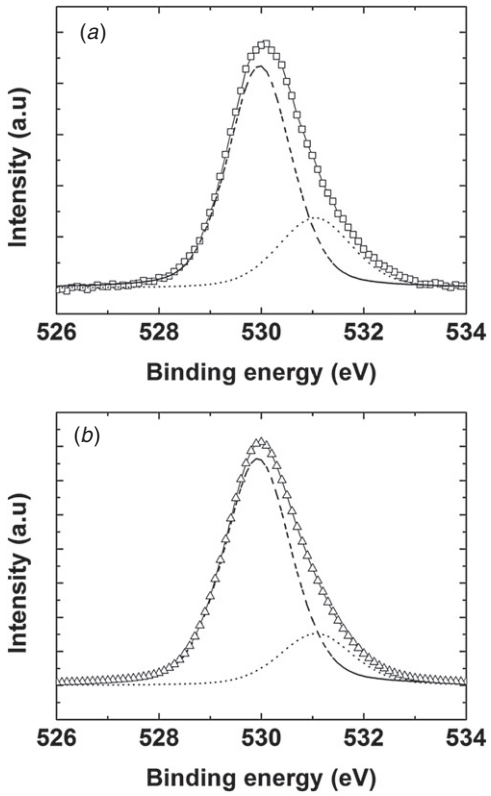

Figure 3. The O 1s XPS spectra of (*a*) ITO TFT 1 and (*b*) ITO TFT 2.

Table 1. The R_C and R_S values of TFTs 1 and 2 at gate voltages of 20 and 30 V.

	Gate voltage = 20 V		Gate voltage = 30 V	
	R_C (kΩ)	R_S (MΩ)	R_C (kΩ)	R_S (MΩ)
TFT 1	6.5	0.12	19.9	0.16
TFT 2	2.4	0.076	5.1	0.101

versus channel length plots of TFTs 1 and 2 at gate voltages of 20 and 30 V. The value of R_T was acquired from the slope of the linear region of the output curve, and the transmission line method (TLM) measurements were performed with three electrode spacings (250, 500 and 750 μm). The contact resistances (R_C) and channel resistances (R_S) were determined from the R_T value by applying the TLM [2]. The R_C and R_S values of TFT 1 at a gate voltage of 20 V were 6.5 kΩ and 0.12 MΩ, respectively, while the R_C and R_S values of TFT 2 increased to 19.9 kΩ and 0.16 MΩ, respectively. The R_C and R_S values of TFTs 1 and 2 at gate voltages of 20 and 30 V are summarized in table 1. It was reported that R_C is lower for a channel layer with high electron concentration [17]. The increases of R_C and R_S affected the reduction of μ_{FE}, on-state current and $I_{on/off}$.

Figure 3 shows the XPS spectra of the O 1s of the ITO thin films after Ar ion sputtering. The binding energies of the core levels were calibrated by setting the C 1s peak to 285 eV. The O 1s peak was decomposed into two components at 530.3 and 531.0 eV, which were associated with In_2O_3 and oxygen-deficient In_2O_{3-x}, respectively [18]. When the O_2 flow rate was increased in the deposition process, the intensity ratio of

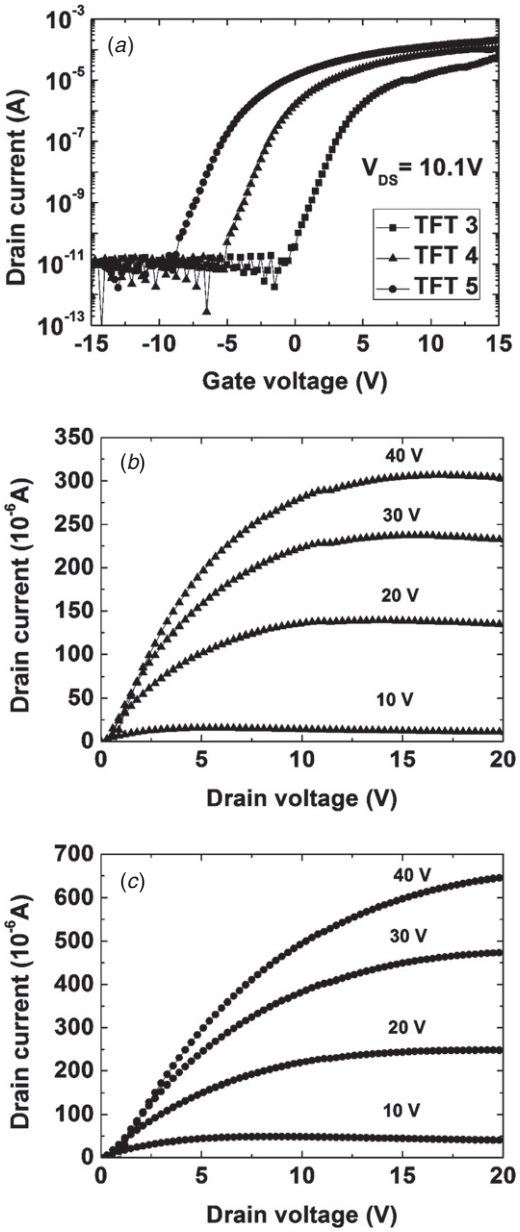

Figure 4. (*a*) The transfer characteristics of the channel-modulated ITO TFTs at a drain voltage of 10.1 V and output characteristics of (*b*) TFT 4 and (*c*) TFT 5.

the oxygen-deficient In_2O_{3-x} decreased from 26.9% to 19.9%. This indicates that the carrier concentration in the ITO thin film decreased at the increased O_2 flow rate.

Figure 4(*a*) shows the transfer characteristics of the channel-modulated ITO TFTs at a drain voltage of 10.1 V. TFT 1 demonstrated a high μ_{FE} of 19.0 cm^2 V^{-1} s^{-1} and a high $I_{on/off}$ of 3.4 $\times$ 10^7 due to the high carrier concentration and low R_C. However, its V_{th} value was negative at −13.1 V. In contrast, TFT 2 has a low μ_{FE} of 4.5 cm^2 V^{-1} s^{-1} and a low $I_{on/off}$ of 1.9 $\times$ 10^6 due to the low carrier concentration and a high R_C, but instead its V_{th} was a positive value of 6.5 V. In order to obtain a high μ_{FE} and moderate V_{th}, channel-modulated TFTs were fabricated. The channel layer of TFT 3 was composed of a low carrier concentration layer and a high concentration layer, as the O_2 flow rate was decreased from 4.5 to 4 sccm

Table 2. The device performance parameters of the ITO TFTs.

	O_2 (sccm)/Thickness (nm)	V_{th} (V)	μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	S_{SUB} ($V\ dec^{-1}$)	$I_{on/off}$
TFT 1	4/25	−13.1	19	1.06	3.4×10^7
TFT 2	4.5/25	6.5	4.5	0.77	1.9×10^6
TFT 3	4.5–5/13–12	3.0	5.7	0.93	3.8×10^6
TFT 4	4–4.5–4/4–17–4	−1.5	9.2	0.95	1.2×10^7
TFT 5	4–4.5–4/8–9–8	−4.4	11.4	0.98	2.1×10^7

during the deposition. V_{th} was shifted to 3.0 V, and the on-state current was increased compared to that of TFT 2. μ_{FE}, S_{SUB} and $I_{on/off}$ increased to 5.7 $cm^2\ V^{-1}\ s^{-1}$, 0.93 $V\ dec^{-1}$ and 3.8×10^6, respectively. The shift of V_{th} was due to the increased carrier concentration in the channel. The increases of μ_{FE}, on-state current and $I_{on/off}$ were affected by the increase of the carrier concentration and the decrease of R_C. The channel layers of TFTs 4 and 5 were composed of a high concentration layer, a low carrier concentration layer and a high concentration layer, as the O_2 flow rate was increased from 4 to 4.5 sccm and then decreased from 4.5 to 4 sccm during the deposition. The thickness of each layer was controlled by the deposition time and the high concentration layers of TFT 5 were thicker than those of TFT 4. This information is summarized in table 2. The V_{th} of TFT 4 shifted to −1.5 V, and the on-state current increased. In addition, μ_{FE}, S_{SUB} and $I_{on/off}$ increased to 9.2 $cm^2\ V^{-1}\ s^{-1}$, 0.95 $V\ dec^{-1}$ and 1.2×10^7, respectively. The V_{th} of TFT 5 shifted to −4.4 V, and the on-state current increased, while the μ_{FE}, S_{SUB} and $I_{on/off}$ values increased to 11.4 $cm^2\ V^{-1}\ s^{-1}$, 0.98 $V\ dec^{-1}$ and 2.08×10^7, respectively. In the TFT 4 and 5 structures, V_{th} was negatively shifted due to the increased carrier concentration in the channel. The increases of μ_{FE}, on-state current and $I_{on/off}$ were due to the high carrier density around the channel/gate insulator interface and the low R_C at the channel/electrode interfaces. Here, the enhanced electrical performance of the TFT device is obtained due to the insertion of a high carrier concentration layer at the channel/gate insulator and channel/electrode interfaces. Figures 4(*b*) and (*c*) show the output characteristics of TFTs 4 and 5, respectively. The channel-modulated TFTs 4 and 5 show a clear pinch-off and excellent drain current saturation behavior with enhancement mode operation, indicating that the channel layer was completely controlled by the gate and drain voltages. The electrical performance parameters of the TFTs are also summarized in table 2.

4. Conclusion

In summary, we fabricated channel-modulated TFTs and analyzed the device characteristics. The channel-modulated TFTs with a high carrier concentration layer at the channel/gate insulator and channel/electrode interfaces resulted in the enhancement of the electrical performance of the TFT because of the increased carrier concentration and reduced parasitic resistance. This arrangement combines the advantage of the double-channel layer structure and the insertion of a high carrier concentration layer between the channel and electrode. Therefore, the TFTs with the modulated channel structure can be applied to transparent and flexible electronics due to their high mobility, moderate threshold voltage and low process temperature.

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