The effect of gate separation on low temperature polycrystalline silicon thin film transistors by mechanical stress

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Abstract — In use of foldable or bending application in display industry, the degradation of thin film transistor (TFT) characteristics can be occurred by the destruction or degradation of the gate electrode. Especially, the destruction of gate electrode can degrade the performance of TFTs since the separated gate electrodes hold the electric field to the channel for activation. In this paper, the effect of separated gate on TFT characteristics by mechanical stress is investigated.

Index Terms — Gate electrode, low temperature polycrystalline silicon thin film transistors

I. INTRODUCTION

For future foldable or flexible display industry, various types of TFTs on flexible substrate is researched recently [1]. Among many promising TFTs, low temperature polycrystalline TFTs are focused due to its high field effect mobility and high driving current. The effect of mechanical stress on these flexible thin film transistors is analyzed to improve its reliability. Previously, the ductility of material for gate electrode was reported [2]. Because material for the gate electrode is usually brittle, the reliability on mechanical stress is poor. For gate electrode separation, the electric field from the gate is captured between the separated electrodes. Thus, the channel gets less electric potential and the TFT characteristic is degraded. In this paper, the effect of separated electrodes is investigated by modeling and simulation using the electric field distribution and the I-V characteristics.

II. SIMULATION

In this paper, ATLAS device simulator (Silvaco) [3] is used to build the TFT model and the electrical parameters are extracted. In this work, the low-temperature polycrystalline silicon (LTPS) is used as active layer of TFT with 50 nm thickness and 100 nm of SiO2 layer is used as gate dielectric. Top gate structure is used for modeling and simulation and 4 different separated lengths of the gate electrode are examined for comparison. The 4 simulated lengths are 20, 50, 100 and 200 nm, respectively.

III. RESULT AND DISCUSSION

A. Simulation result

Fig. 1 shows the crack generated after the mechanical stress on the LTPS TFT. It is observed that the simulated distance of separated electrode was set from 0 to 200 nm.

The I-V characteristics of various separated distances are described in Fig. 2 and they are degraded more as crack width of gate electrode goes wider due to the distribution of electric field from the gate electrode. The electric field distribution with and without crack is shown in Fig. 3. As shown in Fig. 3, the maximum electric field is formed between the separated gate electrodes. Thus, the electric field at the channel region is reduced and eventually less current flows through the channel. Because wider crack captures more electric field, more degradation occurs when wider crack is generated.

B. Field effect mobility extraction

To estimate the effect of separated gate electrode as a value of parameter, the field effect mobility has been extracted from the I-V characteristic and calculated through Eq. 1 [4].

$$\mu_{FE} = \frac{L \cdot g_m}{W \cdot C_i \cdot V_{DS}}$$  (1)

where $V_{DS}$ = 2.1V and $g_m$ is transconductance for linear region. Fig. 4 presents the change in field effect mobility for each separated gate length. As mentioned before, because wider crack captures more electric field, less electric field activates the channel. As a result, $g_m$ in Eq. 1 becomes smaller and eventually degrades the field effect mobility.

IV. CONCLUSION

In this work, the effect of separated gate electrode has been examined through simulation tool. As a result, the destructed gate electrodes blocked the electric field to the channel region, which degrades the transconductance ($g_m$). Degradation in $g_m$ decreased the field effect mobility resulting in the reduction of the driving current as the crack width becomes wider.

REFERENCES

Fig. 1 SEM image of crack on LTPS TFT.

Fig. 2 I-V characteristic of different crack widths.

Fig. 3 Distribution of the electric field at the gate electrode with crack width of (a) 100nm and (b) 0nm.

Fig. 4 Variation of the extracted field effect mobility