In-Situ Threshold Voltage Shift Monitoring of Amorphous InGaZnO Thin-Film Transistors

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Keywords: InGaZnO (IGZO), thin-film transistors (TFTs), modeling, in-situ monitoring

ABSTRACT

Threshold voltage shift ($\Delta V_{th}$) characteristics of amorphous InGaZnO thin-film transistors under positive gate bias stress are investigated and the monitoring $\Delta V_{th}$ from constant current induced drain voltage is proposed. The extracted $\Delta V_{th}$ characteristics are then analyzed using the stretched exponential model and the characteristics of the subgap density of states.

1. INTRODUCTION

Amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) have been studied vigorously as one of the promising candidates for the backplane electronics of large area display applications [1]. Recent researches have tended to focus on instability issues of a-IGZO TFTs such as positive/negative bias temperature stress instability (PBS/NBS) and the characteristic variation under light illumination. Threshold voltage shift ($\Delta V_{TH}$) characteristics have been examined as one of the degradation characteristics which are dominantly induced by variation in the channel-insulator interface or channel bulk trap properties under electrical or optical stress [2]. Typically, time-dependent $\Delta V_{TH}$ are analyzed using the stretched exponential model in which threshold voltage ($V_{TH}$) are extracted intermediate of stress tests [3, 4]. This induces relaxation of trapped charge in the channel under stress tests. Thus, this scheme has a limitation in understanding the changes of channel characteristics with continuous stress condition. For the aim of degradation compensation in the device or circuit characteristics under operational condition, degradation characterization in-situ is required. To achieve this goal, in-situ monitoring method with no relaxation of trapped charge from the interface trapping levels in $V_{TH}$ extraction is necessary [3]. In this paper, $\Delta V_{TH}$ monitoring method of a-IGZO TFT by applying a constant drain current under PBS is proposed. Time-dependent instability characteristics under PBS are modeled using the stretched exponential model. Channel degradation mechanism is also analyzed by density of states (DOS) model using TCAD simulation.

2. FABRICATION AND MEASUREMENT

The test structure has a conventional staggered bottom gate structure with an etch stopper layer (ESL) on an a-IGZO channel thin film with an aspect ratio of W/L = 200 µm/50 µm [5, 6]. A Mo metal gate was sputtered onto a glass substrate, and a 60-nm-thick a-IGZO channel layer was deposited after a 200-nm-thick SiNx insulator layer was formed using plasma enhanced chemical vapor deposition (PECVD) process [5]. Mo source/drain electrodes were then formed on the etch stopper and channel layer. The transfer curves with a low drain field voltage ($V_{DS} = 0.1$ V) and output curves at the gate saturation voltage region ($V_{GS} = 15$ V) were measured as pre-stress characteristics. From the initial output characteristics at the positive gate bias stress voltage of $V_{GS} = 15$ V, the constant monitoring current ($I_{DS\_monitor}$) was 1 µA, which induced a low field drain voltage (drain voltage increased from $V_{DS} = 0.16$ V to $V_{DS} = 0.18$ V) in the linear region while stress test, where $V_{DS} < (V_{GS} - V_{TH})$ according to the output characteristics. Thus, positive gate bias stress was performed with $V_{GS} = 15$ V and constant $I_{DS\_monitor} = 1$ µA to the drain electrode for 3 hours. The threshold voltage was extracted from the conversion equation using measured drain voltage during the stress test. The threshold voltages were extracted intermediate of 1 hour during the stress test by measuring transfer characteristics to compare with the converted threshold voltage. The current-voltage (I-V) measurements of the stress tests were performed using Keithley 236 source measurement units.

3. RESULT AND DISCUSSION

Initial and stressed transfer characteristics at a low drain field ($V_{DS} = 0.1$ V) with stress condition of $V_{GS} = 15$ V is shown in FIG. 1. Initial characteristics showed field effect mobility ($\mu_{FE}$), $V_{TH}$, and subthreshold swing (SS) of 4.42 cm²/V·s, 1.87 V, and 0.3 V/dec, respectively. Instability characteristics under PBS with constant drain monitoring current ($I_{DS\_monitor} = 1$ µA) showed a typical rigid parallel positive $\Delta V_{TH}$ [2]. Here, $I_{DS\_monitor}$ induced drain voltage increased during PBS in the range of the low field region assuming no alter of on channel interface trap generation [7]. Thus, $V_{TH}$ was calculated from measured drain voltage using linear regime equation, $V_{TH} = V_{GS} - \mu_{FE}[I_{DS\_monitor}/W/L]C_{ox}V_{TH}$, where $W/L$, $C_{ox}$, and $\mu_{FE}$ are the channel planar aspect ratio, insulator capacitance per unit area, and field effect mobility, respectively [8]. In this equation, $V_{TH}$ was assumed to be constant as the initial value, and the drain voltage ($V_{DS}$) was considered as $I_{DS\_monitor}$ induced time-varying parameter. Inset of FIG. 2 shows the measured $V_{DS}$ for 3 hours under PBS. Discontinuities were induced from intermediate I-V measurements for the $V_{TH}$ comparison between the

ISSN-L 1883-2490/20/0364 © 2013 ITE and SID

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conventional and proposed $V_{TH}$ characteristics. The calculated $\Delta V_{TH}$ was fitted using the stretched exponential model, $\Delta V_{TH} = \Delta V_{TH0} \{1 - \exp[-(t/\tau)^\beta]\}$, where $\Delta V_{TH0}$ is $\Delta V_{TH}$ at infinite time, is the stretched exponential exponent, and $\tau$ is the characteristic trapping time of the carriers [3]. The extracted stretched exponential model parameters were summarized in Table 1. From the extracted parameters, the characteristic trapping time increased as the stress time increased. To investigate the trapping time characteristics under PBS, the channel trap states were analyzed based on the density of states (DOS) characteristics, which were extracted using ATLAS 2-D simulation (Silvaco Co.) [4]. For the simulation, total carrier density was calculated as $2.12 \times 10^{16}$ cm$^{-3}$ using $N_{T} = C_i V_{on}/q t_c$, where $C_i$, $V_{on}$, and $t_c$ are the gate dielectric capacitance per area, the turn-on voltage, and the channel thickness, respectively [9]. Subgap DOS parameters were extracted using exponential tail state and Gaussian deep state as following equation:

$$g(E) = N_{TA} \times \exp\left[\frac{(E - E_c)}{E_{TA}}\right] + N_{GA} \times \exp\left[\frac{(E - E_c)}{E_{GA}}\right]$$

where $E$, $N_{TA}$, $E_c$, $W_{TA}$, $E_{TA}$, $N_{GA}$, and $W_{GA}$ are trap energy, conduction band (CB) intercept density, CB energy, characteristic decay energy of the tail states, central energy, density at the central energy of the Gaussian distribution (GD), and the characteristic decay energy of the GD, respectively. The extracted variables from the optimization procedure were summarized in Table 2. From the results, the decrease in the density of the acceptor-like donor state dominantly affected the decrease of $\tau$ of the stretched exponential model. The initial DOS parameters were in a valid range with applied low-field transfer characteristics which were reported previously in several papers [10, 11]. The increases of the Gaussian states and the characteristic decay energy induced the positive $V_{TH}$. FIG. 3 shows the optimized subgap DOS characteristics for the transfer curves in the experiment range from $V_{GS} = 0$ V to $V_{GS} = 20$ V with $V_{DS} = 0.1$ V (Here, the Fermi level in the channel varies in the range from $E_F$ to ($E_c - 0.8$) eV). Here, the calculated Fermi level at $V_{GS} = 15$ V was $~0.04$ eV. Thus, the calculated unoccupied trap from $E_c$ to $E_F$ decreased from $2.14 \times 10^{16}$ to $1.0 \times 10^{15}$ cm$^{-3}$ as the stress time was increased. Thus, the decrease of the characteristic trapping time was due to the decrease of unoccupied trap states. The measured and simulated transfer curves using the extracted subgap DOS model were shown in FIG. 4. The inset of FIG. 4 shows the comparison of $V_{TH}$ between the conventional extrapolation method and the proposed scheme. $V_{TH}$ characteristics from the proposed procedure showed consistency with conventional $V_{TH}$ characteristics. The errors seem to come from ambiguity in the conventional $V_{TH}$ extraction method and the conversion error of the proposed scheme under constant parameter assumptions. The proposed $V_{TH}$ estimation scheme has an advantage in monitoring channel degradation characteristics with no relaxation of trapped charges for device or circuit characteristics compensation. Moreover, the understanding of a channel degradation mechanism under continuous PBS condition is introduced using the conventional DOS and the stretched exponential model.

4. CONCLUSION

Real-time threshold voltage shift monitoring scheme was performed using the measured constant drain current-induced drain voltage. The time-dependent threshold voltage shift characteristics under a positive gate bias stress were well explained by the proposed drain voltage conversion procedure, which was compared to the conventional linear extrapolation method-based stretched exponential model. The increase of the trapping characteristic time of the stretched exponential model under stress was analyzed based on the subgap DOS characteristic using the ATLAS 2-D simulation. In addition, the increase of the electron capture characteristic time was found to be due to the decreases in the unoccupied trap states, which were calculated from the simulated subgap DOS characteristics at the stress conditions.

ACKNOWLEDGEMENT

This work was supported and funded in part by the research project of LG Display.

REFERENCES


Table 1. Stretched exponential model fitting parameters

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<th>Stress time (s)</th>
<th>( \tau ) (s)</th>
<th>( \beta )</th>
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<tr>
<td>3600</td>
<td>( 7.19 \times 10^1 )</td>
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<tr>
<td>7200</td>
<td>( 2.09 \times 10^4 )</td>
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</tr>
<tr>
<td>10800</td>
<td>( 4.19 \times 10^4 )</td>
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Table 2. Summary of extracted subgap DOS parameters for intermediate transfer characteristics under gate bias stress test

<table>
<thead>
<tr>
<th>Time (sec.)</th>
<th>( N_{TA} ) (cm(^{-3})/eV)</th>
<th>( W_{TA} ) (eV)</th>
<th>( N_{GA} ) (cm(^{-3})/eV)</th>
<th>( W_{GA} ) (eV)</th>
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<tr>
<td>0</td>
<td>( 5.43 \times 10^{17} )</td>
<td>0.146</td>
<td>( 5.85 \times 10^{16} )</td>
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</tr>
<tr>
<td>3600</td>
<td>( 4.12 \times 10^{17} )</td>
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<td>( 6.13 \times 10^{16} )</td>
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<td>7200</td>
<td>( 1.93 \times 10^{17} )</td>
<td>0.577</td>
<td>( 6.88 \times 10^{16} )</td>
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</tr>
<tr>
<td>10800</td>
<td>( 1.63 \times 10^{17} )</td>
<td>0.672</td>
<td>( 9.17 \times 10^{16} )</td>
<td>1.103</td>
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Fig 1. Transfer characteristics and threshold voltage extraction using the linear extrapolation method under positive gate bias stress. (The sweep was performed at \( V_{DS} = 0.1 \) V.)

Fig 2. Threshold voltage shift according to the linear equation and fitted result using the stretched exponential equation. Inset shows sequentially measured drain voltages under bias conditions of \( V_{GS} = 15 \) V with \( I_{DS} = 1 \) \( \mu \)A for 3 hours.

Fig 3. DOS plot with a Fermi level sweep range.

Fig 4. Measured and simulated transfer curves using the extracted subgap DOS model. (inset) Comparison of threshold voltage shifts under gate bias stress between the linear extrapolation method and the proposed scheme.