Effects of Type and Density of Interface trap in Tunneling Oxide for Flash Memory Devices

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Abstract— As the device size in the chip shrinks, shrinking the size of the insulators including tunneling oxide and the inter-poly dielectric is mainly focused on the memory devices. However, the degradation of reliability of insulators is also induced as decreasing the size of chip. In case of flash memory, especially, operation principle is cycling of electrons between floating gate and substrate. So, the degradation is easily caused by the traps caused by tunneling at interface and generation of leakage path through tunneling oxide as scaling down. In this paper, the effects of the trap density and the type of trap at the interface in tunneling oxide are analyzed by using the change of the simulated current density through the tunneling oxide using TCAD model.

Keywords-Flash memory, interface trap, Degradation, Tunneling oxide, Barrier lowering, Fowler-nordheim tunneling, TCAD.

I. INTRODUCTION
In flash memory, the degradation of reliability is very important problem since the principle of flash memory is electrons storage system [1]. Thus, the tunneling oxide and the ONO inter-poly dielectric (SiO$_2$-Si$_3$N$_4$-SiO$_2$) insulator sandwiched with the floating gate are very important factors to associate with the degradation of device because the characteristics of insulators are related with the leakage current mechanism. Specifically, the tunneling oxide is very important role to operate the flash memory due to the cycling operation of electron for the flash memory [1]. When we perform the program or erase cycle, the electron moves between floating gate and substrate through tunneling oxide by fowler-nordheim tunneling [4]. So, they induce the degradation of tunneling oxide. Recently, researches related to degradation of tunneling oxide are studied in various bias and temperature stress conditions [2-4]. These stress conditions generate interface traps and fixed charges to Si/SiO$_2$ and poly-Si/SiO$_2$ interfaces nearby tunneling oxide [3], and these induce the degradation of reliability. However, they do not know where the traps are generated and what type of trap is generated and affected the variation of current-voltage (I-V) characteristics. To analyze these effects, in this paper, we simulate the effect of the interface trap density and types of the trap by inserting traps to interfaces nearby the tunneling oxide using the our tunneling oxide model by TCAD simulation is based on the measurements of the experimental I-V characteristics.

II. EXPERIMENTS
The experiment to verify our simulation of tunneling oxide I-V characteristics is performed by fabricating the stacked ONO layer as test structures. The I-V characteristics of the test structures were measured to extract the leakage current when it is operated as an erase operation which is defined as the negative voltage applied to the floating gate.

III. SIMULATION METHODOLOGY
In order to analyze the effect of the traps, the I-V characteristics of the tunneling oxide layer was simulated using Synopsys Sentaurus TCAD program and compared with the measured data. The substrate of our structure was p-type silicon layer, and we deposited tunneling oxide and poly silicon layer. Then, we implanted the arsenic atom followed by the annealing process. As a model, the fowler-nordheim tunneling mechanism was dominant leakage mechanism of tunneling oxide for the simulation [4]. To know the effects of type of interface trap, we changed the types of the interface trap for the simulation. We inserted the neutral electron trap sites and neutral hole trap sites to Si/SiO$_2$ and poly-Si/SiO$_2$ interfaces because these trap sites were generally generated under a bias, which is typical for the operation of flash memory [3]. The neutral electron trap site was only electrons can moves into this site and the neutral hole trap site was only holes can moves into this site. We also changed the trap density to Si/SiO$_2$ and poly-Si/SiO$_2$ interfaces.

IV. RESULTS AND DISCUSSION
At first, based on our simulation results, the neutral electron trap sites were only effective to poly-Si/SiO$_2$ interface and the neutral hole trap sites were ineffective at this interface. This reason is that our floating gate was the n-type poly silicon layer. A number of electrons from the floating gate are larger than a number of holes from the substrate since a few holes are tunneling through the tunneling oxide. Therefore, the dominant effect was generated by trapped electrons nearby the poly-Si/SiO$_2$ interface and these trapped electrons changed the I-V characteristic of tunneling oxide. In case of the Si/SiO$_2$ interface, only the neutral hole trap sites were effective factor...
by similar principle. Holes from the substrate which is p-type silicon layer were more trapped to this interface than electrons from the floating gate through tunneling oxide and it was previously discussed that anode hole trapping requires less energy and can occur with thin oxide structure [5]. Therefore, many researchers discover only positive charges at the anode/oxide interface which is the Si/SiO₂ interface under negative gate voltage stressing.

Now, we changed the effective trap density at each interface. We gradually changed the neutral electron trap density at poly-Si/SiO₂ interface, and also we changed the neutral hole trap density at Si/SiO₂ interface. The leakage current level variations according to the electric field at each interface were presented in Fig. 1 and Fig. 2. Here, as the effective trap sites are increased, the current level also increases by trapped charges at low electric field because these trapped charges produce the internal field nearby the interface [3]. When electrons moves from the floating gate to the neutral electron trap sites at poly-Si/SiO₂ interface, this leads to a negative surface charge density at the interface and the increase of the electron concentration at the interface. So, it induced the bending energy band of the tunneling oxide at the interface.

Since the dominant carrier of test structures was an electron, the additional electrons were tunneling by using the fowler-nordheim mechanism through the part at poly-Si/SiO₂ interface which is locally thin by bending energy band of the tunneling oxide. In case of Si/SiO₂ interface, additional electrons were tunneling through the locally thin energy band of poly-Si/SiO₂ interface by positive trapped charge density. However, the current density has not much variation until a number of neutral density reaches $10^{15}$/cm². Thus, we empirically found that the lower bound of neutral electron trap density to affect the leakage current density is around $10^{13}$/cm².

As shown in Fig. 2, there were little different point at Si/SiO₂ interface. When we simulated the case for the neutral hole trap density as many as $10^{15}$/cm², the current density was increased to the level when the neutral hole trap density is larger than $10^{13}$/cm² at only low electric field. However, the current density of both hole neutral trap densities of $10^{15}$/cm² and $10^{14}$/cm² were almost the same when the electric field is larger than $7 \times 10^6$ V/cm. When we inserted the more neutral trap sites to Si/SiO₂ interface, the more electric field was required to have the same current density in high electric field region. It indicates that the hole trapping at low electric field to Si/SiO₂ interface was gradually annihilated by the injected tunneling electrons from the floating gate [6]. The more trap sites were existed, the larger electric field was required to annihilate the additional trapped holes.

V. CONCLUSION

The effect of the types and density of interface trap nearby tunneling oxide was investigated using the TCAD simulation to analyze the degradation mechanism of tunneling oxide by the interface traps. It was found that the hole neutral trap sites were dominant factor at anode-oxide interface and the electron neutral trap sites were dominant factor at cathode-oxide interface. In addition, as the neutral trap density was increased, the leakage current density was also increased by barrier lowering effect of trapped charge and we also empirically found that the effective trap density to affect leakage current was larger than $10^{17}$/cm².

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REFERENCES