Effects of Alternating Pulse Bias Stress on Amorphous InGaZnO Thin Film Transistors

S. Park, E. N. Cho, and I. Yun

Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Republic of Korea

Amorphous InGaZnO (a-IGZO) TFTs attracted more demands due to the transparency and high mobility. Since TFTs are always exposed to both positive and negative gate bias, the alternating pulse bias stress tests are required to ensure stable TFT characteristics. In this paper, the effects of alternating pulse bias stress on the threshold voltage shift ($\Delta V_{th}$) of a-IGZO TFTs with respect to the channel length ($L$) and the stress time interval ($T_{interval}$) are investigated using the concepts of the stretched-exponential function and the density of total trap states ($N_T$).

Introduction

Transparent ZnO based thin-film transistors (TFTs) have many advantages including the advantage of low temperature fabrication using glass substrate and flexibility. Amorphous InGaZnO (a-IGZO) TFTs attracted more attention because of their large drain current ($I_{DS}$) on-off ratio and high mobility (1), (2). In practical applications, because TFTs are generally used for switching, they are always exposed to both positive and negative gate bias ($V_{GS}$). Several papers investigated the effects of positive and negative gate bias stress independently (3), (4). However, the effects of both positive and negative gate bias stresses in a sequence were rarely investigated (5). Moreover, the issue of how frequently the sign of gate bias stress changes not using the AC bias is not yet studied. In this paper, +20V and -20V $V_{GS}$ stresses were alternatively applied in a sequence during same total stress time ($T_{stress}$), total positive stress time, and total negative stress time, but with the different stress time interval ($T_{interval}$). The transfer characteristics ($I_{DS}$–$V_{GS}$) were measured to investigate the electrical stability including the variation of threshold voltage ($\Delta V_{th}$), and subthreshold swing ($\Delta S_{SUB}$). The variations of electrical performance of IGZO TFTs are analyzed with respect to frequency of the alternating DC gate bias stresses.

Experiments

The a-IGZO TFT test structures were fabricated on a glass substrate with 250-nm-thick Mo gate metal deposited by sputtering. The 200-nm-thick SiNx gate insulating layer was deposited on the gate by plasma enhanced chemical vapor deposition (PECVD). The 40-nm-thick IGZO layer was deposited by sputtering using a polycrystalline $\text{In}_2\text{Ga}_2\text{ZnO}_7$ target. The channel width ($W$) of TFTs was fixed at 100 $\mu$m and the channel lengths ($L$) were varied with 25 $\mu$m, 50 $\mu$m, and 100 $\mu$m. The total stress time was the same for the three stress conditions. The three sets of stress conditions each have stress time interval ($T_{interval}$) as 10 (Set 1), 20 (Set 2), and 40 (Set 3) minutes as shown in Fig. 1. They have total 40-minute positive stress time and total 40-minute negative stress time.
The transfer characteristics ($I_{DS}$-$V_{GS}$) of TFTs when drain voltage ($V_{DS}$) equals 2.1V and 10.1V were measured during the stress tests using Keithley 236 source measure unit. $V_{th}$ was extracted by linear extrapolation of $I_{DS}$-$V_{GS}$ curve in the range of 90%–10% of the maximum $I_{DS}$ (6).

![Figure 1. Alternating DC bias stress conditions: (a) Set 1, (b) Set 2, and (c) Set 3.](image)

**Results and Discussion**

Figure 2 shows the measured initial and final transfer curves for IGZO TFTs within possible combination of two $V_{DS}$ conditions (2.1 V and 10.1 V) and three stress sets (S1, S2, and S3) with 100-μm-thick channel width and 25-μm-thick length. As the same trend of the analysis of Suresh et al. (3), $I_{DS}$-$V_{GS}$ curve shifted to the right with amount of $\Delta V_{th}$ when the positive gate bias was applied. On the other hand, $I_{DS}$-$V_{GS}$ curve slightly shifted to the left when the negative gate bias was applied. Prior to investigate the effect of $T_{interval}$, the feasibility of the results is conducted. Figure 3 represents the comparison of $\Delta V_{th}$ with respect to L with different stress conditions. As shown in Fig. 3, the variations of $V_{th}$ under three stress sets were always higher than $\Delta V_{th}$ under $V_{GS}$ stress of -20 V during 80 minutes and were always lower than $\Delta V_{th}$ under $V_{GS}$ stress of +20 V during 80 minutes.
Figure 2. Measured initial (squared) and final (star) transfer curves for IGZO TFTs with W=100 μm and L=25 μm: (a) Set 1 (VDS=2.1V), (b) Set 1 (VDS=10.1V), (c) Set 2 (VDS=2.1V), (d) Set 2 (VDS=10.1V), (e) Set 3 (VDS=2.1V) and (f) Set 3 (VDS=10.1V).
Figure 3. The comparison of $\Delta V_{th}$ with respect to $L$ with different stress conditions.

Relationship between $L$ and $\Delta V_{th}$. Figure 4 represents $\Delta V_{th}$ with respect to $T_{interval}$ with different channel length when $V_{DS}$ are (a) 2.1 or (b) 10.1 V. Based on the results, $\Delta V_{th}$ is length-dependent under the alternating pulse bias stress. $\Delta V_{th}$ increases as $L$ decreases from 100 $\mu$m to 25 $\mu$m.

Figure 4. $\Delta V_{th}$ with respect to $T_{interval}$ with different $L$: (a) $V_{DS}=2.1$ V and (b) $V_{DS}=10.1$ V.

One of the reasons to explain the length-dependent tendency for $\Delta V_{th}$ is verified by carrier trapping parameters extracted from the stretched-exponential function. We attribute $\Delta V_{th}$ to the charge injection from the IGZO channel into traps between the channel/dielectric interface or in the gate insulator. The experimental data on $\Delta V_{th}$ is well described by the stretched-exponential function. The stretched-exponential function for $\Delta V_{th}$ is explained as a function of $T_{stress}$ by (7), (8):

$$
\Delta V_{th} = \Delta V_{th0}[1 - \exp\{-(t / \tau)^\beta\}]
$$

where $\Delta V_{th0}$ is $\Delta V_{th}$ at infinite time, $\tau$ is the characteristics trapping time of carriers, and $\beta$ is the stretched-exponential exponent. Figure 5 shows the $T_{stress}$ dependency of $\Delta V_{th}$ for only gate bias stress of 20V with varying channel lengths. The scattered points represent the measured $\Delta V_{th}$ while the straight lines represent the stretched-exponential model for $\Delta V_{th}$ with fixed $\beta$ ($=0.68$) (9). Two parameters, $\Delta V_{th0}$ and $\tau$, are extracted. $\Delta V_{th0}$
increases from 3.24 V to 3.83 V as L shrinks down. τ decreases from 3374 s to 1028 s as L decreases from 100 μm to 25 μm. Since τ is related with the effective barriers for carriers in channel to overcome before they enter the trap sites, smaller τ causes the shorter charge trapping time; therefore, short channel induces more charge trapping than the long channel and also induces bigger ΔV_{th} than the long channel (8), (10).

Figure 5. ΔV_{th} versus T_{stress} for 20 V gate bias stress with different channel lengths. The scattered points represent the measured ΔV_{th} while the straight lines represent the stretched-exponential model for ΔV_{th} with fixed β (=0.68).

Another reason why ΔV_{th} increases as L shrinks down is supported by the difference of the density of total trap states (N_T) caused by the different subthreshold swing (S_{SUB}). S_{SUB} was determined by:

\[ S_{SUB} = \frac{dv_{GS}}{d(\log I_{DS})} \]  

[2]

The density of deep bulk states (N_{bulk}) and the density of defects at the interface between channel and insulator (N_{it}) compose N_T and can determine N_T as a function of S_{SUB} by following equation (11), (12):

\[ N_T = N_{bulk} + N_{it} = \left( S_{SUB} \log(e) \frac{C_{ox}}{kT/q} - 1 \right) \frac{C_{ox}}{q} \]  

[3]

where e is the Euler’s number, k is the Boltzmann constant, T is the absolute temperature, q is the charge of an electron, and C_{ox} is the gate insulator capacitance per unit area. According to Eq. (2), the average S_{SUB} values after total 80 minutes when V_{DS}=10.1 V and W=100 μm with different L is shown in Fig. 6. Each error bar represents the standard deviation among the tested TFTs with the same channel length. As L decreases, there is an apparent increment of S_{SUB} induced by the drain-induced barrier lowering (DIBL) phenomenon. As DIBL literally leads to lowering of the barrier for current conduction between the channel and source, it causes the degradation due to scaling-down of TFTs including the increased S_{SUB} (13). Since S_{SUB} increases from 0.58 V/decade to 0.72 V/decade, N_T also increases from 1.86×10^{12} /cm^{3} to 2.35×10^{12} /cm^{3} when L decreases.
from 100 μm to 25 μm. It is reasonable to interpret bigger \( N_T \) as more carriers being trapped.

\[ \Delta V_{th} \] is obtained by the following equation, as a linear function of \( N_T \) (6):

\[
\Delta V_{th} = q \frac{N_T}{C_{ox}}
\]  \[4\]

From Eq. (4), the calculated \( \Delta V_{th} \) increases when \( N_T \) increases due to the increasing \( S_{SUB} \). Therefore, shorter channel causes the bigger \( S_{SUB} \), and also causes the higher number of trapped charge, and finally induces the bigger variation of \( V_{th} \).

![Figure 6. The average \( S_{SUB} \) values after total 80 minutes when \( V_{DS}=10.1 \) V and \( W=100 \) μm with different \( L \).](image)

**Relationship between \( T_{interval} \) and \( \Delta V_{th} \).** As shown in Figure 4, \( \Delta V_{th} \) is increased as \( T_{interval} \) decreases from 40 minutes to 10 minutes. It is quite reasonable to interpret the alternating pulse bias as combination of the AC +20V bias stress with 50% duty and the AC -20V bias stress with 50% duty. Fung et al. reported the phenomenon that \( \Delta V_{th} \) of alternating pulse bias is approximately equal to the adding up the \( \Delta V_{th} \) values under AC +20V and AC -20V bias stress cases (9). Therefore, Set 1 is considered as the combination of AC +20V and AC -20V bias stress with 1/1200Hz pulse bias frequency. Likewise, Set 2 has 1/2400 Hz and Set 3 has 1/4800 Hz pulse bias frequency. As \( T_{interval} \) corresponding to the AC pulse width decreases from 40 minutes to 10 minutes, the alternating pulse bias frequency corresponding to the AC bias frequency increases from 1/4800 Hz to 1/1200 Hz. The experimental result shows that \( \Delta V_{th} \) is frequency-dependent. Several studies indicated that the higher frequency induces the higher \( \Delta V_{th} \) under positive AC stress due to the charge trapping at the interface between channel and dielectric (9), (14). Therefore, the high-frequency stress can impact on the device characteristic degradation more severe than the low-frequency stress.

**Conclusion**

The effects of alternating pulse bias stress on a-IGZO TFTs with three different lengths of 25, 50, and 100 μm were analyzed by using the concepts of the stretched-
exponential function and the density of total trap states. The $V_{GS}$ stresses of +20 V and -20 V were alternatively applied in a sequence during the same total stress time, total positive stress time, and total negative stress time, but with different stress time interval. $\Delta V_{th}$ increases as L decreases from 100 $\mu$m to 25 $\mu$m due to the increment of $N_T$, and as $T_{interval}$ decreases from 40 minutes to 10 minutes due to increased pulse bias frequency. Thus, the devices stressed with long $T_{interval}$ showed more stable properties. Therefore, it was shown that long channel is more reliable than short channel when the devices are exposed to both positive and negative gate bias stress.

References