Frequency-dependent Characterization of Multi-finger MOSFETs with Different Gate Structures

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Abstract

As the scaling down of MOSFETs, the prediction of the device performance and behavior becomes more complicated. The parasitic components critically affect to the device characteristics especially for the high-frequency region. Thus, the models for the DC and high-frequency characteristics of MOSFETs are required to predict the device performance and improve the device characteristics. In this paper, Berkeley short-channel insulated gate field effect transistor model 4 (BSIM4) is used to build an equivalent circuit model via the measured data for multi-finger MOSFETs fabricated using the Samsung 130-nm process. The test-structure of the multi-finger MOSFETs with different gate structure are used to characterize their frequency-dependent behavior. The extracted parameters from the equivalent circuit model are analyzed and compared with previously investigated TSMC 0.35-um device to investigate the effect of parasitic components.

INTRODUCTION

For several years, many research groups and companies have worked on the scaling down of MOSFET devices to integrate more devices and functions in the same chip area. This is the way to accomplish to fabricate the low-cost devices. Multi-finger MOSFET is one of the candidates since the device can have the performance of large scaled device and the gate controllability is higher than the small scaled device [1].

However, with the scaling down of the MOSFETs, there are a lot of problems such as a parasitic effect that can affect to the performance of device at high-frequency region significantly [2]. Therefore, there have been many research efforts to reduce the parasitic effect by changing structure of devices. Based on this trend, the modeling technique using technology computer-aided design (TCAD) is getting more important because those can make expect the performance of novel structure of devices and evaluate it before the manufacturing stage. Equivalent circuit modeling is one of the modeling techniques that model the device as a circuit which contains the parasitic components near the device [3]. Based on the core model, BSIM4 model in this study, the parasitic components such as resistors, capacitors, and inductors are connected to each terminal of the core model. Each on the components stands for the parasitic elements that exist in MOSFET itself, connecting line, and the pad for measurement. The values of the components are extracted by parameter optimization using the measured data and the characteristics of device are then analyzed using the model.

Experiments

Test structures of single n-MOSFETs are used for the modeling scheme. The MOSFETs which have the finger width (Wf) of 2, 4, and 6 µm while the number of fingers is fixed with 4 fingers is used as test structures. A total width (Wt) is calculated by multiplying the number of fingers and finger width.

![Figure 1 standard structure of multi-finger MOSFET (N_f=4)](image)

The basic structure of multi-finger MOSFET is schematically shown in Figure 1 and the sample sets
used for this experiment are also summarized in Table 1.

<table>
<thead>
<tr>
<th>Table 1 Summary of geometric information for test structures</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_f (\mu m) )</td>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>( N_f )</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

There are 3 samples (S1, S2, and S3) to observe the variations of gate width are examined. Therefore, three samples are used to analyze the tendency of multi-finger MOSFETs from gate finger structure variations which is the gate finger width.

The equivalent circuit models for the test structures of MOSFETs are built using BSIM4 core model and several parasitic components. The BSIM 4 core is not well agreed with the measured data for the test structures, especially for the magnitude of \( S(2,1) \) parameter. Therefore, the K1 factor which is the one of the parameter in the core model related to the first order body effect is tuned [4]. Figure 2 shows the diagram for the equivalent circuit model.

![Figure 2 the equivalent circuit model used for parameter extraction](image)

The pad parts are constructed by simple partial element equivalent circuit (PEEC) method using \( C_{gpad}, R_{gpad}, \) and \( C_{gpad} \) for gate pad and \( R_{dpad}, C_{dpad}, \) and \( C_{dpad} \) for drain pad. The resistor named \( R_g, R_d, R_s, \) and \( R_b \) are connected to each terminal of the core model and the rest of parasitic components are placed in designated location of the model. From this structure, the pad values are fixed using deembedding patterns and then optimize the rest values using advanced design system (ADS) tool. After the parameters are extracted, transconductance \( (g_m) \) and transit frequency \( (f_T) \) or intrinsic cut-off frequency which are important parameters to estimate the performance of MOSFET at high-frequency region, are calculated using below equations [1, 5]:

\[
g_m = \left. \frac{\partial I_d}{\partial V_{GS}} \right|_{v_{sat}} = |Y(2,1) - Y(1,2)|
\]

(1)

The transconductance is calculated from \( Y \)-parameter as shown in equation (1). From the measured S-parameters, the \( Y \)-parameter can be calculated using the function of ADS as follows:

\[
f_T = \frac{g_m}{2\pi C_{gin} \sqrt{1 + 2 \frac{C_{miller}}{C_{gin}}}} \approx \frac{f_c}{\sqrt{1 + 2 \frac{C_{miller}}{C_{gin}}}}
\]

(2)

The transit frequency can be calculated after the transconductance is obtained. \( C_{miller} \) is a capacitance that reflects the miller effect, and \( C_{gin} \) stands for the gate input capacitance. The values are calculated with the following equations:

\[
C_{gin} = C_{gs} + C_{gs0}, \quad C_{miller} = C_{gd} + C_{gd0}
\]

(3)

In these equations, \( C_{gs0} \) and \( C_{gd0} \) is the capacitance of gate to source and gate to drain at zero bias. These values are calculated by the following equation:

\[
C_{gd0} = C_{gs0} = -\frac{\text{Im} [Y_{12}]}{\omega}
\]

(4)

The test structures are measured using HP4145B Semiconductor Parameter Analyzer for DC characteristics and Agilent 8722 Vector Network Analyzer for high-frequency characteristics. The optimization is performed using ADS tool.

**Results and Discussion**

From the modeling results, the values of parasitics are extracted and summarized in Table 2. After the optimization, the S1 to S3 DC results are shown in Figure 3. As the Figure 3 shows, optimized circuit can explain the DC characteristic of test samples. Using this optimization, the parasitic resistances which are connected to the drain, source, bulk, and gate are extracted. After the extraction of the resistances,
optimization for RF characteristics is done by adjusting capacitances and inductances while the resistances are fixed with the values. Then the values of capacitors and inductors can be extracted from the optimization result.

### Table 2 Extracted model parameters for test structures.

<table>
<thead>
<tr>
<th></th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_s$ (Ω)</td>
<td>112.1</td>
<td>58.9</td>
<td>34.6</td>
</tr>
<tr>
<td>$R_g$ (Ω)</td>
<td>19.4</td>
<td>16.2</td>
<td>12.8</td>
</tr>
<tr>
<td>$C_{gd}$ (fF)</td>
<td>1.09</td>
<td>6.02</td>
<td>21.4</td>
</tr>
<tr>
<td>$C_{ds}$ (fF)</td>
<td>196</td>
<td>200</td>
<td>189</td>
</tr>
<tr>
<td>$C_{gs}$ (fF)</td>
<td>229</td>
<td>198</td>
<td>173</td>
</tr>
<tr>
<td>$C_{jd}$ (fF)</td>
<td>5.02</td>
<td>5.07</td>
<td>14.9</td>
</tr>
<tr>
<td>$C_{js}$ (μF)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

The samples named S1, S2, and S3 have different gate widths while the number of gate fingers is fixed. As the finger width is increased, the saturation drain current is increased because the total gate width is increased. The equivalent circuit models this phenomenon as the source resistance decrease. This is the reason that the source resistance of S1 is larger than the source resistance of S3. However, the drain resistances have constant value of $10^6$ Ω because the source resistance works as the current controller. The gate resistance is involved to the gate structure because the resistance is related to the total gate width. Therefore, the gate resistance is decreased as the total gate width is increase. In addition, the gate finger width increase is modeled with increased gate-drain capacitance ($C_{gd}$) and drain junction capacitance ($C_{jd}$). The other values are maintained at similar level for the case of S1, S2 and S3.

The capacitance increment is due to the coupling effect which is elevated when the gate structure has more complex structure. The metal line of gate affect to the near gate metal and vice versa. When the interference is occurred, parasitic capacitive coupling is originated and the energy within the metal line is transferred. The simulator catches this phenomenon from the measured data of the samples and models it as a capacitance increment. The results of RF optimization for S1 are shown in below Figure 4.

![Figure 4 S-parameter modeling results for test structure S1](image)

In the Figure 4, the symbols stand for the optimized values and strict line shows the measured value of S-parameter real value. The dotted line in the figure is measured value of S-parameter imaginary value. The real value of equivalent circuit for S1 is well fitted to the measured data as shown in Figure 4. However, the error exists with $S(2,1)$ optimization because of the K1 factor tuning. Initially, the core model has a problem of $S(2,1)$ magnitude modeling. The tuning reduces the magnitude error significantly but it still cannot make exact fitting. In spite of the error, the model can follow measured data for every frequency range. Figure 4 shows only for the S1, but the other test samples are all optimized using same method as the similar error range. From the optimization, the capacitance values shown in table 2 are extracted.

Based on this complete equivalent circuit, the transconductance and the transit frequency can be easily calculated. The transconductance comparison is shown in Figure 5 using equation (1).
Figure 5 The comparison of transconductance and transit frequencies for test structures

As the finger width is increased, the transconductance is increased. Using this parameter extraction and characteristic calculations, a device designer can choose the structure in limited area shape with same performance target.

Using the results from transconductance calculation, transit frequency can be calculated with equation (2). The consequence is shown in Figure 5, as well. The transit frequency has similar tendency to the transconductance because the values are calculated from the transconductance. However, the C_miller and C_gin are different in the aspect of its variation gap between samples.

Compared to the previous work of Yim et al. [1] the transconductance and transit frequency are much smaller due to the dimension of the device. The transconductance of the previous work shows the variation from 0.032 to 0.045. However, in this study, the transconductance is varying from 0.003 to 0.014. As the gate dimension is scaled down to 130-nm, the gate resistance is significantly increased compared to the gate resistance of 350-nm MOSFET [1]. Moreover, the total width of previous work is varying from 250 – 300 um but, in this experiment, the total width is varying from 8 um to 24 um. Thus, the variation of the transconductance is much smaller than the result of previous work [1]. In case of the transit frequency, the similar tendency can be found due to the scale of the gate structure [6].

However, the transconductance and transit frequency are nearly constant with respect to the measured frequency range indicating that the MOSFETs have not much degradation at high frequency region compared to the large scale devices.

Conclusion

The equivalent circuit for 130-nm multi-finger MOSFETs with gate finger width variation was established. The circuit can model the behavior of multi-finger MOSFETs with parasitic elements and BSIM4 core model. Using this model, the transconductance and transit frequency can be calculated. The MOSFET characteristics with gate finger width variation were compared with the previous results of the 350-nm MOSFETs. As a result, the MOSFETs exhibit stable performance regardless of the frequency range. The equivalent circuit model can also provide the information about each parasitic components variation.

References