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Impact of bias stability for crystalline InZnO thin-film transistors

Hojoong Kim,1,2 Daehwan Choi,1,2 Solah Park,1,2 Kyung Park,2 Hyun-Woo Park,3 Kwun-Bum Chung,3 and Jang-Yeon Kwon1,2,a)
1School of Integrated Technology, Yonsei University, Incheon 406-840, South Korea
2Yonsei Institute of Convergence Technology, Yonsei University, Incheon 406-840, South Korea
3Division of Physics and Semiconductor Science, Dongguk University, Seoul 100-715, South Korea
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Crystallized InZnO thin-film transistors (IZO TFTs) are investigated to identify a potential for the maintenance of high electrical performances with a consistent stability. The transition from an amorphous to a crystallization structure appeared at an annealing temperature around 800 °C, and it was observed using transmission electron microscopy and time-of-flight secondary ion mass spectrometry analysis. The field-effect mobility of the crystallized IZO TFTs was boosted up to 53.58 cm²/V s compared with the 11.79 cm²/V s of the amorphous devices, and the bias stability under the negative stress was greatly enhanced even under illumination. The defect states related to the oxygen vacancy near the conduction band edge decreased after the crystallization, which is a form of electrical structure evidence for the reliability impact regarding the crystallized IZO TFTs. Published by AIP Publishing. [http://dx.doi.org/10.1063/1.4985295]

The oxide semiconductor thin-film transistors (TFTs) form a huge branch in the field of active matrix displays and diodes due to its attractive properties of a reasonable electrical mobility, transparency for visible light, and low fabrication costs.1–3 However, an instability issue regarding the voltage-bias stress and which accelerated under illumination has persisted in terms of the general use of the oxide material in technology. The general origins of the bias instability are known as the defect creation, charge trapping, vacancy ionization, and environmental conditions.4,5 The bias stress generates or traps carriers inside the channel or at the interface between the channel and the gate insulator, resulting in the threshold voltage ($V_{TH}$) shift. The ionization of the oxygen vacancy ($V_O$) under illumination creates electron carriers, thereby accelerating the $V_{TH}$ shift. Last, the moisture and oxygen in air can also affect the channel level so that it makes passivation treatment or structural modification necessary. A high electrical mobility can be expected for the In contained ZnO semiconductor due to the high carrier density in the In, while simultaneously generated defects also degrade the device stability.6,7 The doping of a carrier suppressor such as Zr, Hf, and Ga into the semiconductor can stabilize the defect level for the development of device reliability, but most carrier suppressors also reduce the electrical mobility.8,9

A previous study reported the c-axis aligned crystal InGaZnO (CAAC-IGZO) TFTs as an effective source of the negative bias illumination.10,11 The CAAC-IGZO decreased the defect level at the deep bandgap states more than the amorphous IGZO, even maintaining its electrical characteristics. In spite of the IGZO crystallization without the axis orientation, a high temperature annealed crystallization can also reduce the defect level and enhance the device stability.12 It is understood that the defect level in the sub-conduction band is effectively diminished by the crystallization; therefore, the simple annealing process for crystallizing the oxide semiconductor can be an alternative to the preservation of the reliability without a deterioration of its initial characteristics. Even though the IGZO is a credible material for many applications, the limitation on electrical mobility at around 10 cm²/V s shows that a higher conductive oxide is still required. Consequently, crystallizing InZnO (IZO) TFTs have a potential in terms of the maintenance of a high electrical mobility with reliability among the other oxide materials.

In this study, amorphous IZO TFTs are transformed into the crystal phased devices by high temperature annealing. The phase variation of the IZO thin film is identified as a function of the annealing temperature, and the electrical characteristics and stability of both devices are compared through an electrical structure based analysis.

The amorphous IZO TFTs were fabricated as the bottom-gate structure on a highly doped P-type Si wafer through the use of a 100 nm thermally grown SiO$_2$ as a gate insulator. The IZO thin film (In:Zn = 7:3) was deposited as an active channel layer using radio frequency (RF) sputtering with a sputter power of 100 W and an oxygen partial pressure (O$_2$/O$_2$ + Ar) of approximately 9.1% under 5 mTorr of working pressure. A lift-off technique was exploited for patterning the channel layer with a width/length area of 200 μm/50 μm through photolithography. An alpha step measurement identified the channel thickness as 50 nm. To crystallize the IZO thin film, a post-channel annealing was progressed for 1 h in a tube furnace with a varying temperature of 600 °C, 800 °C, and 1000 °C. Mo electrode of 150 nm was deposited as a source and drain contact using sputtering, and last, all devices were heated at 200 °C for 1 h to reduce the contact resistance.

To identify the crystal structure of the IZO thin films depending on the annealing temperature, X-ray diffraction (XRD) patterns were measured as a function of post-channel annealing temperature ($T_p$), which is shown in Fig. S1 (supplementary material). Up to 600 °C, XRD peak of the IZO does not show any particular peak intensity that is related to the IZO. While at a further $T_p$ increment at 800 °C, the diffraction peaks of (211), (222), and (400) as the In$_2$O$_3$ crystal
were investigated. Figure 3(a) shows the transfer curves of IZO thin film, the electrical characteristics of the IZO TFTs state after the TP transformation from the amorphous to the polycrystalline patterns also show the definite evidence of the IZO phase enlarged images of the TP. Alternatively, a clear crystalline shape is identifiable in the morphology variation is not appeared as increasing TP. The IZO and the SiO2 are discovered in the images over face undulation on the IZO and a shallow interlayer between the IZO and SiO2 is relatively distinguishable at the as-dep (a) IZO did not grow any further with raising temperature. The images at the downside of each bright-field image show the high magnification focus of the IZO film, and the insets indicate the selected area electron diffraction (SAED) patterns of the IZO. In the bright-field images of as-deposition (as-dep) and TP = 600 °C annealed samples, the morphology variation is not appeared as increasing TP. Following the crystallization confirmation, the IZO film composition variation was investigated owing to the morphology degradation after the 800 °C as shown earlier. The graphs in Figs. 2(a)–2(d) are the depth profiles from the IZO to the SiO2 measured by the time-of-flight secondary ion mass spectrometry (TOF-SIMS). The interface between the IZO and SiO2 is relatively distinguishable at the as-dep (a) and TP = 600 °C states (b), while the Zn ion in the IZO film is diffused into the SiO2 layer after the TP = 800 °C (c). The diffusion caused a reduction of Zn composition ratio in the IZO, and created a layer with higher amount of In. The compositional variation was advanced as the Zn diffusion deeply penetrated into the SiO2 layer at the TP = 1000 °C (d). After the identification of the structural changes in the IZO thin film, the electrical characteristics of the IZO TFTs were investigated. Figure 3(a) shows the transfer curves of the IZO TFTs as a function of the TP with a 10 V of drain-source voltage (VDS). The transfer characteristic of the as-dep IZO device demonstrated a typical semiconducting curve shape with the field-effect mobility (µFE) of 11.79 cm2/V s, the VTH of 18.68 V, and the subthreshold swing (SS) of 0.41 V/dec. The µFE defined by transconductance (gm) was calculated by the following equation: 

\[ g_m = \frac{W}{L} \frac{C_{ox} \mu_{FE}}{V_{DS}} \tag{1} \]

where the \( g_m \) is the gradient of the transfer curve, \( W/L \) is the ratio of the channel width and length, and \( C_{ox} \) is the capacitance per unit area of the gate insulator. The µFE at the maximum value of the \( g_m \) was represented as the electrical mobility. The transfer curve of the as-dep IZO TFTs was changed to a constant line shape after 600 °C due to the higher electrical conductivity of the channel by the electron carrier generation. As the TP approached to 800 °C, the conductive channel was retransformed to the semiconductor, predicted as a consequence of the channel crystallization. The variation of the electrical conductivity could be the result of the diminution of the VO in the amorphous channel by the IZO crystalline arrangement. The device parameters of the µFE, VTH, and SS at 800 °C were calculated to 53.58 cm2/V s, 8.31 V, and 0.58 V/dec, respectively. The significant µFE boost could be owing to the variation of the channel composition ratio, which is caused by the high In amount in the semiconductor. Lastly at the TP = 1000 °C, the transfer curve was negatively shifted by the creation of the electron carrier, and the values of the µFE, VTH, and SS were 46.34 cm2/V s, -1.86 V, and 0.96 V/dec, respectively. The degradation of the µFE and SS could be originated from the severe deformation of the channel and interfacial layers by the extreme annealing temperature. The device parameters at each TP are summarized in Table I. The electrical reliability as the variation of the film phase structure was investigated. The as-dep and TP = 800 °C IZO TFTs were selected as the amorphous and crystalline devices for evaluating under the bias stress. The test was implemented inside a dark chamber under the vacuum condition to minimize the environmental effects from the air. The stress test was carried out until 7200 s and the measurement interval was set to 600 s. A gate-source voltage (VGS) of −40 V and
the $V_{DS}$ of 10 V were applied for the negative bias stress (NBS), and $V_{DS} = 40$ V and $V_{DS} = 10$ V for the positive bias stress (PBS). The transfer curve of the as-dep IZO TFTs under the NBS was gradually shifted to the negative side. Whereas which of the 800°C annealed device was slightly moved to the positive side within relatively early test time. The parallel shift of the transfer curve under the NBS was attributed to the donor-like trap states by the gate electric field. The trap states at the IZO/SiO$_2$ interface were shifted by the NBS upon the Fermi level so that the traps donate charges to the conduction band. On the other hand, the trap sites in IZO TFTs were eliminated by the crystallization, which reduced the negative $V_{TH}$ shift under NBS. The sudden positive shift of $V_{TH}$ revealed that new charge trapping sites could be created in the crystallized IZO TFTs and capture electrons during the measurement. The electron trapping at the interface between the channel and the gate insulator or at the grain boundary inside the channel could be attributed to the positive $V_{TH}$ shift even under the NBS. A similar phenomenon was reported on the poly-Si TFTs. The electrons trapped and fixed into the defect sites can also erase the defect density, and as a consequence, the SS characteristic was significantly improved in the first 1200 s of the NBS. The gate voltage movement at the 1 nA drain current ($\Delta V_{\text{inA}}$) in the as-dep device was approximately $-16.0$ V. In the case of the PBS, the evolution at the as-dep IZO TFTs shows a gradual movement to the positive side with a degradation of the SS value, while they remained stationary for most of the stress time at the $T_p = 800$ °C. In the next phase, the NBS and PBS under illumination (NBIS and PBIS) were performed with a white LED light of 290 lux. The negative shifting of the as-dep curves was drastically increased under the NBIS compared to the NBS by the

<table>
<thead>
<tr>
<th>Post-annealing temperature ($T_p$)</th>
<th>as-dep</th>
<th>800 °C</th>
<th>1000 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu_{FE}$ (cm$^2$/V s)</td>
<td>11.79</td>
<td>53.58</td>
<td>46.34</td>
</tr>
<tr>
<td>$V_{TH}$ (V)</td>
<td>18.68</td>
<td>8.31</td>
<td>-1.86</td>
</tr>
<tr>
<td>S.S (V/dec)</td>
<td>0.41</td>
<td>0.58</td>
<td>0.96</td>
</tr>
</tbody>
</table>

FIG. 2. TOF-SIMS depth profiles of the IZO thin films at each $T_p$: (a) as-dep, (b) 600 °C, (c) 800 °C, and (d) 1000 °C.

FIG. 3. Electrical characteristics of the IZO TFT devices. (a) Transfer curves of the TFTs as a function of the post-annealing temperature at $V_{DS} = 10$ V. (b) The evolution of the transfer curves under the bias-stress tests summarized as the gate voltage movement at the 1 nA drain current.
assistance of the illumination. After crystallization, however, the $\Delta V_{\text{inA}}$ was decreased from $-34.6$ V to $-5.4$ V, and this reduction ratio was much larger than that under the NBS test (even though the positive shift at the $T_p=800$ °C was included). It means that the $V_O$ ionization accelerated by the illumination was also decreased. Therefore, it leads to the possibility that the defect states which corresponding to the diminution of the $V_O$ was decreased after the crystallization of the IZO TFTs. It is also noticeable that the $T_p=800$ °C under NBIS showed SS reduction. Decreasing SS could explain the elimination of trap site on the interfaces or the channel grain boundary during the measurement as similar to the NBS test. The movement of the transfer curves under the PBIS was relatively comparable to that under the PBS for both devices. The $\Delta V_{\text{inA}}$ under all of the stress tests is summarized in Fig. 3(b), and Fig. S3 (supplementary material) shows the evolution of the transfer curves under the bias stress tests.

In addition, a similar report has been published regarding the stability of the IZO crystallization. Oh et al. fabricated IZO TFTs by varying the composition ratio of In and Zn. An increasing of the In content in the polycrystalline ZnO transformed the IZO film into the amorphous phase. As the phase variation, the device stability was simultaneously degraded whereas the electrical characteristics were improved. They mentioned that the In weakened the crystal structure of the ZnO and created the $V_O$, which showed a lower stability in the IZO TFTs with the high In amount. In our study, the bias stability of the crystalline IZO TFTs was enhanced with the high In concentration, which is regarded for the possibility of high performance devices with an excellent stability in terms of the crystallized oxide TFTs.

For a further investigation in a perspective of the electronic structures, a systematic spectroscopic analysis was performed in the beamline 2A of Pohang Acceleration Lightsource. Figure 4(a) shows the normalized O K1 edge X-ray absorption spectroscopy (XAS) spectra of the as-dep and post-annealed IZO and the second derivative O K1 edge spectra are respectively at the bottom of the graph. (b) The band edge states over a narrow energy region below the conduction.

The electrical mobility was greatly improved in the crystallized devices due to the compositional variation and the phase transformation, which were mainly oriented by the In$_2$O$_3$, respectively. The reduction of the vacancy defects that are located near the conduction band edge supports the origin of the stability in the crystalline phase. Crystallization is potentially an effective reliability solution, even in the highly defective semiconductors, for the increasing of the electrical performances.

See supplementary material for the characterization of the IZO films by XRD and XPS. Output curves of IZO TFTs and the evolution of transfer curves under the stress tests are also included.

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FIG. 4. (a) The normalized XAS O K1 edge spectra of the as-dep and 800 °C post-annealed IZO and the second derivative O K1 edge spectra are respectively at the bottom of the graph. (b) The band edge states over a narrow energy region below the conduction.

See supplementary material for the characterization of the IZO films by XRD and XPS. Output curves of IZO TFTs and the evolution of transfer curves under the stress tests are also included.

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