The Impact of Device Configuration on the Photon-Enhanced Negative Bias Thermal Instability of GaInZnO Thin Film Transistors

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We investigate the effect of device configuration on the light-induced negative bias thermal instability of gallium indium zinc oxide transistors. The Vth of back-channel-etched (BCE)-type transistors shifted by ~3.5 V, and the subthreshold gate swing (SS) increased from 0.88 to 1.38 V/decade after negative bias illumination temperature stress for 3 h. However, etch-stopper-type devices exhibited small \( V_{th} \) shifts of ~0.8 V without degradation in the SS value. It is believed that the inferior instability of the BCE device is associated with the formation of an interfacial molybdenum (Mo) oxychloride layer, which occurs in the course of dry etching Mo using Cl2/O2 for source/drain patterning.

We have investigated the effect of device configuration on the light-induced negative bias thermal instability of gallium indium zinc oxide (GIZO) thin film transistors (TFTs) that involve the formation of an etch stopper layer that protects the channel during the source/drain etch process. However, the SS value of the BCE back surface is vulnerable to plasma damage when dry-etch processes are used for source/drain (S/D) formation, which results in undesired carrier trap generation in the exposed channel surface. Another detrimental effect of plasma damage is the induction of a conductive channel back surface owing to the apparent increase in oxygen vacancy concentration.6,7 To avoid these unfavorable consequences of dry etching, using an ES layer to protect the channel may be a better solution for the fabrication of pristine TFT devices.

Because the switching transistors of AM-LCD devices are always subjected to light exposure and pulsed gate voltage stress during operation, systematic investigations on their stability under negative bias illumination thermal stress (NBITS) are necessary to guarantee their application into viable products.

In this article, we report the influence of the device structure on the light-induced negative bias thermal instability (NBITS) of GIZO TFTs. The bottom-gate structures of BCE and ES types were fabricated and compared in terms of the light-induced NBITS. The stability of the BCE-type device under the NBITS condition is inferior to that of the ES-type device, which may be attributed to the formation of an unfavorable interfacial layer (such as MoOx/Clx) between the GIZO channel and the SiOx passivation during the dry-etching process of the Mo S/D electrode.

Experimental

Two kinds of bottom-gate gallium indium zinc oxide TFTs were fabricated as follows: first, sputter-deposited Mo was patterned by photolithography and subsequent wet etching on glass substrates to form the gate. Then, 400 nm thick SiOx gate insulator films were deposited by plasma-enhanced chemical vapor deposition (PECVD). Next, 70 nm thick amorphous indium gallium zinc oxide (a-IGZO) layers were grown by radio-frequency sputtering and patterned by photolithography and wet etching. In the BCE structure, the S/D patterns were formed by dc-sputtering Mo, followed by photolithography, and reactive ion etching (RIE) using Cl2/O2 chemistry. However, in the ES structures, 200 nm thick SiOx films were grown by PECVD and patterned by dry etching before depositing the Mo S/D electrode. After patterning the S/D on both devices, 200 nm thick SiOx was deposited as a passivation layer by PECVD. The schematic cross sections of bottom-gate TFTs with (a) BCE and (b) ES configurations are shown in Fig. 1. Finally, the sample was annealed in air at 200°C for 1 h. The electrical characterization of a-IGZO TFTs was carried out using a Keithley 4200-SCS parameter analyzer, which is composed of a heating stage and a halogen lamp. A white light of a halogen lamp was used as the photon source. The experiments were performed in a N2 glove box to eliminate the influence of oxygen molecules or moisture on the bias stability of the devices.

Results and Discussion

Figure 2a and b shows the evolution of the transfer curve as a function of the applied negative bias illumination temperature stress (NBITS) time for the BCE and ES structures, respectively. The devices were stressed under the following conditions: the \( V_{GS} \) and \( V_{SD} \) were fixed to ~20 and 10 V, respectively, at a measurement temperature of 60°C. During the stress evaluation, the illumination on the device surface and the total stressing time were 180 lm/m² and 3 h. The field-effect mobility (1.4–1.8 cm²/V s) and \( I_{on}/I_{off} \) ratio (>10) were observed to be similar in both devices before the stressing experiment. The transfer curve of the BCE device exhibits a stretch-out in the subthreshold drain current region (10⁻⁸–10⁻¹³ A) as well as a large negative \( V_{th} \) shift with increasing stress time. However, the ES device exhibits a much smaller change in \( V_{th} \) in the negative direction without any degradation in the subthreshold drain current. Figure 3a and b shows the parameter variations in the subthreshold gate swing (SS) and \( V_{th} \) values as a function of the NBITS time for both devices. The initial SS of the BCE device is associated with the formation of an interfacial molybdenum (Mo) oxychloride layer, which occurs in the course of dry etching Mo using Cl2/O2 for source/drain patterning.

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The back interfacial structure was evaluated by transmission electron microscopy (TEM). Figure 4a and b shows cross-sectional TEM images for the BCE and ES structures, respectively. A thin and rough interfacial layer in the BCE device is formed between the active channel and passivation. TEM images for the BCE and ES structures, respectively. A thin and smooth interfacial layer in the BCE device is formed between the active channel and passivation.

The chemical and structural properties near the back surface of the GIZO channel layer for both devices were then studied in detail. The back interfacial structure was evaluated by transmission electron microscopy (TEM). Figure 4a and b shows cross-sectional TEM images for the BCE and ES structures, respectively. A thin and rough interfacial layer in the BCE device is formed between the active channel and passivation (see Fig. 4a), whereas in the ES structure, a smooth and clean interface structure is observed without any secondary by-product in between (Fig. 4b). From the energy-dispersive spectroscopy analysis, it was found that molybdenum and chlorine are present in the interfacial layer, suggesting that this undesired by-product may have formed during the RIE process of the Mo S/D electrode using Cl₂ chemistry.

The chemical binding state of the interfacial layer was further characterized by high resolution X-ray photoelectron spectroscopy (XPS). Figure 5a shows the Mo 3d and Cl 2p XPS spectra of the dry-etch-related interfacial layer, respectively. The binding energy split in the Mo 3d peak suggests that the layer is composed of mainly MoO₂ with a small amount of MoCl₃. In addition, the Cl 2p XPS spectra show the coexistence of compounds such as ZnClₓ, InClₓ, and MoClₓ.

Figure 1. (Color online) Schematic cross section of the GIZO TFTs (W/L = 70/20 μm), which have an inverted staggered bottom-gate structure with (a) BCE and (b) ES configuration.

Figure 2. (Color online) Evolutions of the transfer curves as a function of the applied NBITS time for the (a) BCE and (b) ES configurations.

Figure 3. (Color online) Parameter variations in the SS and Vₜh values for the (a) BCE and (b) ES configurations. For comparison, the variations in the Vₜh values for both devices without light illumination under the identical stress condition were included in (b). The Vₜh values were evaluated at the gate voltage inducing the Iₛₛ of L/W × 10⁻⁸ A and the SS values [SS = dV₋₁₀/d log Iₛₛ (V/decade)] were extracted from the average linear portion of the log Iₛₛ vs Vₛₛ plot in the drain current range from L/W × 10⁻⁸ to L/W × 10⁻⁶ A.

Figure 4. (Color online) Cross-sectional TEM image of the (a) BCE and (b) ES configurations. The insets of each (a) and (b) are a higher magnification picture of the SiOₓ passivation/GIZO interface in the BCE and ES structures, respectively.

Figure 5. (Color online) (a) Mo 3d and (b) Cl 2p XPS peak of the film containing the dry-etch-related interfacial by-product layer.
Based on the above observations, the inferior stability of the BCE device in the light-induced NBTTI is believed to result from the RIE process of the Mo S/D electrode. Although the exact mechanism for the light-enhanced $V_{th}$ shift under the negative gate-bias condition is not fully understood at present, a possible mechanism may be suggested as follows. Obviously, the negative $V_{th}$ shift cannot be attributed to the electron trapping at the channel/gate insulator interface because the electron trapping results in the positive $V_{th}$ shift. It is tentatively assumed that the negative $V_{th}$ shift would come from the hole carrier trapping at the channel/gate insulator and/or injection into the gate dielectric bulk film where the inverted hole carrier is caused by the applied negative gate voltage stress. However, it is also expected that the number of hole carriers in the negative gate voltage stress condition is extremely small because there are huge subgap density of states ($>10^{23}/$cm$^3$) near the valence band of the GIZO film. This is why the dark stability under the same gate-bias condition is much better than the stability with light illumination. Now, if the light is irradiated on the oxide TFT device, the large amount of electron–hole pairs is created via the band-to-band transition. The photoinduced electron carrier would be repelled into the back channel by the applied negative gate voltage, which is subsequently moved to the drain electrode because the $V_{DS}$ of 10 V is applied during the NBTTIS. In contrast, the photogenerated hole carrier is accumulated at the channel/gate insulator due to the attractive coulombic force, which can be trapped at the interfacial trap sites or injected into the underlying gate dielectric film. This may constitute the reason for the TFT with light illumination that suffered from much more enhanced $V_{th}$ shift compared to that without light illumination under the same bias condition.

With a viewpoint of the suggested mechanism, it can be explained that the BCE device exhibited the inferior stability against the application of NBTTIS. The defective layer that contains the dry-etch by-products onto the GIZO layer during the patterning process of the S/D electrode. Although the exact mechanism for the light-enhanced $V_{th}$ shift under the negative gate-bias condition is not fully understood at present, a possible mechanism may be suggested as follows. Obviously, the negative $V_{th}$ shift cannot be attributed to the electron trapping at the channel/gate insulator interface because the electron trapping results in the positive $V_{th}$ shift. It is tentatively assumed that the negative $V_{th}$ shift would come from the hole carrier trapping at the channel/gate insulator and/or injection into the gate dielectric bulk film where the inverted hole carrier is caused by the applied negative gate voltage stress. However, it is also expected that the number of hole carriers in the negative gate voltage stress condition is extremely small because there are huge subgap density of states ($>10^{23}/$cm$^3$) near the valence band of the GIZO film. This is why the dark stability under the same gate-bias condition is much better than the stability with light illumination. Now, if the light is irradiated on the oxide TFT device, the large amount of electron–hole pairs is created via the band-to-band transition. The photoinduced electron carrier would be repelled into the back channel by the applied negative gate voltage, which is subsequently moved to the drain electrode because the $V_{DS}$ of 10 V is applied during the NBTTIS. In contrast, the photogenerated hole carrier is accumulated at the channel/gate insulator due to the attractive coulombic force, which can be trapped at the interfacial trap sites or injected into the underlying gate dielectric film. This may constitute the reason for the TFT with light illumination that suffered from much more enhanced $V_{th}$ shift compared to that without light illumination under the same bias condition.

With a viewpoint of the suggested mechanism, it can be explained that the BCE device exhibited the inferior stability against the application of NBTTIS. The defective layer that contains the dry-etch by-products onto the GIZO layer during the patterning process of the S/D electrode. Therefore, the dry etching of the S/D electrode of BCE devices should be carefully done to prevent the formation of the undesired interfacial layer.

## Conclusion

In summary, the device deterioration of the BCE and ES devices under the application of NBTTIS was compared. Although the BCE-type device exhibited a large negative shift ($≈3.5$ V) in $V_{th}$ and degradation in the SS value, the ES device showed a much better $V_{th}$ stability ($≈0.8$ V) without any deterioration in the SS value, indicating no trap creation. These results suggest that the BCE device is more susceptible to the creation and subsequent trapping and/or injection of photoinduced hole carriers, which would be attributed to the formation of MoO$_2$Cl$_2$ by-products. Therefore, it is determined that the ES configuration offers better gate-bias thermal stability against light exposure because the SiO$_2$ ES layer prevents the plasma-induced damage and suppresses the formation of interfacial by-products onto the GIZO layer during the patterning process of the S/D electrode.

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## References