Influence of Illumination on the Negative-Bias Stability of Transparent Hafnium–Indium–Zinc Oxide Thin-Film Transistors

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Abstract—The stability of transparent hafnium–indium–zinc oxide (HIZO) thin-film transistors (TFTs) was investigated under negative-bias stress conditions. TFTs that incorporate transparent electrode materials such as indium–tin oxide or indium–zinc oxide were studied, and the bias stress experiments showed that transparent TFTs undergo severe degradation (negative shift in threshold voltage $V_T$) with simultaneous exposure to white light, in comparison with the results obtained in dark. The time evolution of $V_T$ indicates that the deterioration under illumination occurs mainly by the trapping of photogenerated carriers near the HIZO/dielectric interface.

Index Terms—Hafnium–indium–zinc oxide (HIZO), negative bias illumination stress, thin-film transistor (TFT), transparent display.

I. INTRODUCTION

Oxide semiconductors such as ZnO or GaInZnO (GIZO) are currently subject of intensive research owing to their high potential for application as transparent thin-film transistors (TFTs) [1]–[6]. These can be implemented as driving or switching elements in transparent active matrix organic light-emitting diode (LED) (AMOLED) products, and a potential application may involve a see-through AMOLED panel incorporated into a touch-screen portable phone. The latter will allow the user to access both sides of the screen as two independent touch pads that exhibit distinct functions, thereby offering a more versatile user interface.

In order to ensure the proper implementation of oxide-based TFTs into commercial goods, their stability under prolonged operation must be guaranteed. The switching TFT of an operating AMOLED display is most of the time experiencing a negative gate bias (maintaining the “OFF” state of the n-type transistor, which, in general, lasts more than 500 times longer than the “ON” state). In addition, the devices are inevitably exposed to ambient light in a transparent panel, so it is important to examine and improve their stability under simultaneous application of a negative gate bias and visible light.

While some studies on the bias stability of oxide semiconductor TFTs in dark have recently been reported [7], [8], relatively few investigations on the influence of light are available in the literature [9]–[13], where zinc–tin oxide, IZO, ZnO, and GIZO devices were studied. The addition of light to negative gate bias stress was found to accelerate the degradation (negative shift of the threshold voltage), and the main degradation mechanism was found to consist of charge trapping near the semiconductor/dielectric interface. In the latter studies, either the effect of light only with no gate bias was examined [10], [11] or single-wavelength light sources were employed [12]. Because the aforementioned do not necessarily mimic real operating conditions or environments, in this letter, the effect of white-light radiation on the negative-bias illumination stress of transparent hafnium–indium–zinc oxide (HIZO) TFTs is investigated for the first time. This material has recently been developed by Kim et al. [14] and has successfully been incorporated into high-performance TFTs.

II. EXPERIMENTAL PROCEDURE

The devices were fabricated by evaporating a 200-nm-thick indium–tin oxide (ITO or InSnO) gate and subsequently growing a 400-nm-thick SiO$_2$ dielectric by plasma-enhanced chemical vapor deposition (PECVD). The 70-nm-thick active HIZO layer was formed by radio-frequency sputtering. A 200-nm-thick SiO$_2$ etch stopper layer was then deposited by PECVD, then a 200-nm-thick IZO was sputtered to form the source–drain electrodes. A final protective PECVD SiO$_x$ film was grown, with thickness of 200 nm. All patterning was done by photolithography and appropriate use of wet or dry etching. The aforementioned devices were then annealed in air for 1 h at 250 °C. Fig. 1 shows a diagram of the transparent inverted–staggered bottom-gate TFT and how the measurements were done with the application of a backlight. Devices with width/length = 70/20 μm were characterized using a Keithley 4200-SCS parameter analyzer, and the subthreshold swing ($S$) and saturation field-effect mobility ($\mu_{FE}$) were extracted in compliance with the gradual channel approximation.

Here, the threshold voltage ($V_T$) is defined as the gate voltage that induces a drain current of 1 nA, which is an important reference regarding pixel switching. An LED backlight unit was used to provide white light of specific brightness. The spectrum has a lower end of 410 nm and an upper end of 750 nm.
Fig. 1. Cross-sectional diagram of the transparent TFT and the measurement scheme.

The devices were stressed with a negative gate bias ($V_g = -20$ V and $V_d = 10$ V), and when illuminated, a brightness of 1000 cd/m$^2$ was used. The latter is more intense than typical OLED emissions (in the range of 300–500 cd/m$^2$) [15] and corresponds approximately to the brightness of ambient light in the laboratory where the experiments were carried out. For each stability measurement, a fresh device was used, and the transfer curves were collected every hour for a total duration of 12 h.

III. RESULTS AND DISCUSSIONS

Initial measurements in dark yielded $\mu_{FE} = 8.11$ cm$^2/(V \cdot s)$, $V_T = 0.48$ V, and $S = 0.21$ V/dec.

When the TFT was subjected to negative-bias stress with no light [Fig. 2(a)], the transfer curves exhibited parallel shifts, and the threshold voltage moved only by 0.73 V in the negative direction. The addition of a 1000 cd/m$^2$ white light to the negative-bias stress resulted in a large $V_T$ shift ($\Delta V_T$) of $-10.6$ V [Fig. 2(b)]. At first, the $S$ value seems to increase over time when light is present, which may be indicative of defect generation near the HIZO/dielectric interface. However, the $\mu_{FE}$ does not degrade (which is expected to decrease owing to carrier scattering at interfacial defects), and once the light is turned off, $S$ recovers to the initial value measured in dark. Therefore, the change in $S$ is attributed to the excess photocarriers contributing additional subthreshold current, and it is more reasonable to deduce that the $V_T$ shift occurs by charge trapping at the HIZO/dielectric boundary.

The time evolution of $V_T$ in the stressed devices was then examined, as shown in Fig. 3. The relationship between $\Delta V_T$ and time was found to fit the stretched-exponential model, which describes well the phenomenon of charge trapping in the vicinity of the semiconductor/dielectric interface [12], [16].

The stretched-exponential function is defined as [17]

$$|\Delta V_T| = |\Delta V_{T0}| \left(1 - \exp \left(-\left(\frac{t}{\tau}\right)^\beta\right)\right)$$

where $\Delta V_{T0}$ is the $V_T$ shift at infinite time, $\beta$ is the stretched-exponential exponent, and $\tau$ reflects the characteristic trapping time of carriers. The plots shown in Fig. 3 were fitted accordingly, and the solid lines represent the corresponding extrapolations. The associated parameters are listed in Table I.

It is important to note that the values for $\tau$ and $\beta$ are comparable between the two devices under negative-bias stress with and without illumination, whereas a significant difference is noticed in $\Delta V_T$ and $\Delta V_{T0}$. The values of $\tau$ and $\beta$ are indicative of how easily carriers can be injected into the gate insulator near the semiconductor/dielectric interface, and from the earlier results, it can be concluded that the addition of light itself does not substantially stimulate the rate of charge trapping under identical negative-bias stress. Instead, the considerable difference in $\Delta V_T$ or $\Delta V_{T0}$ between the nonilluminated device and the one exposed to light is presumed to arise from the large concentration of photoinduced holes in the latter, hence providing an abundant pool of carriers to become trapped near the HIZO/dielectric boundary.

In order to minimize the $V_T$ shift, it is thus imperative that the generation of photocarriers be suppressed within the
HIZO bulk. For sputtered oxide semiconductors, the effects of chamber pressure [18], plasma energy [19], and substrate temperature [9] are reported to have a significant influence on the quality of the grown film and, therefore, on the stability of the resulting device. For instance, growth at lower chamber pressures [18] and higher substrate temperatures [9] resulted in structurally denser semiconductor layers. The corresponding TFT devices exhibited characteristics of lower bulk-defect concentrations [18] and smaller $V_T$ shifts under the application of negative bias and light [9]. Relatively lower plasma energies during the sputter process induced less damage and so, lower defect densities near the semiconductor/dielectric interface [19] and so allowed the fabrication of high-quality devices. It is anticipated that optimization of the aforementioned deposition parameters will also help in growing denser less defective HIZO films and hence, diminish their sensitivity with respect to visible-light radiation.

IV. CONCLUSION

In this letter, the stability of transparent bottom-gate HIZO TFTs has been investigated under negative gate bias stress with and without exposure to white light of 1000-cd/m$^2$ brightness. The addition of light on negative-bias stress was observed to accelerate the $V_T$ shift, and the respective time-evolution analyses suggest that such degradation occurs primarily by the increased number of photoinduced hole carriers being trapped near the HIZO/dielectric interface. The susceptibility of the device to light radiation indicates that rigorous efforts must be made in the future to develop oxide semiconductors that are highly stable with respect to illumination, which will allow the realization of transparent display.

REFERENCES


