The Effect of Passivation Layers on the Negative Bias Instability of Ga–In–Zn–O Thin Film Transistors under Illumination

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Gallium indium zinc oxide (GIZO) is an oxide semiconductor that is presently a subject of intensive research as a promising candidate material that can substitute amorphous silicon (a-Si) in thin film transistors (TFTs). Devices that employ GIZO as the active semiconductor exhibit high field effect mobility and high on-off ratio compared to their a-Si counterpart, and the substance can be deposited with reasonable uniformity over large areas. Soon, GIZO TFTs will play a key role in the mass production of large screen ultradefinition liquid crystal displays (LCDs) that necessitate high mobility switching and transistor units. However, in addition to the excellent device properties, to implement GIZO-based TFTs into commercial products, it is imperative that their stability under prolonged operation be guaranteed. Because the TFTs in operating LCD products are most of the time experiencing a negative gate bias to maintain the “off” state of the pixels and are also exposed to light emanating from the backlight unit underneath, the degradation of the device properties by the above situations must be suppressed so as to promote a reasonable lifetime. Thus, the evaluation of TFTs under negative bias illumination temperature stress (NBITS) conditions is necessary to determine what parameters might help to improve their stability.

GIZO transistors are known to degrade primarily by the trapping of a positive charge at the semiconductor/gate insulator, which induces negative shifts in the threshold voltage ($V_{th}$) while exerting a negative gate bias stress. However, provided a gate insulator of reasonable quality, the reliability of GIZO devices then strongly depends on the ability of the passivation to protect the semiconductor from external contamination. Water or oxygen molecules that diffuse through the protective film down to the GIZO film generate additional donor states and induce severe threshold voltage shifts even without the application of a bias stress. The coupling effect of NBITS and humidity accelerates the degradation of GIZO TFTs. Therefore, the most important criterion for a suitable passivation film is its effectiveness in suppressing the penetration of external moisture and oxygen molecules, which are detrimental with respect to device characteristics and stability. A solid passivation structure that can suppress the permeation of water molecules and oxygen can thus effectively improve the GIZO device reliability.

In this article, the influence of different passivation systems on the reliability of GIZO TFTs is studied. The lifetime of GIZO devices can be greatly improved by the selection of appropriate protective layers. In addition, for the device with a relatively porous passivation, the threshold voltage shift ($\Delta V_{th}$) is observed to be governed by two different mechanisms. Donor generation at the lower quality semiconductor/passivation interface dominates the short-term NBITS, and the diffusion of external molecules through a relatively porous passivation, which adsorb onto the GIZO surface, dominates at longer stress times.

GIZO TFTs employing three different passivation structures were fabricated as follows. One sample was covered with only a single silicon oxide ($SiO_x$) layer deposited at a substrate temperature of 150°C (device I). The second type (device II) used a first $SiO_x$ layer deposited at 150°C and a $SiN_x$ film was subsequently grown onto it at 350°C. The last type (device III) had for passivation a first SiO$_x$ film and a second $SiN_x$ layer, both deposited at 350°C. Each device was subjected to NBITS in a relatively humid ambient (with relative humidity = 60%) for 12 hours and the change in threshold voltage with respect to stress time was examined.

During the illumination stress test, the illumination from a white halogen lamp on the device surface was fixed to 180 lumen/m$^2$. The devices were stressed under the following conditions: The gate-source voltage ($V_{GS}$) and drain–source voltage ($V_{DS}$) were fixed to −20 and 10 V, respectively. The details of the device fabrication were described in a previous article.

Figure 1 shows the schematic diagrams of inverted staggered bottom-gate GIZO TFTs. The etch-stopper structure of the device configuration was fabricated in these experiments because in a conventional back-channel-etch structure, a molybdenum oxychloride layer is formed between the active and source/drain, which could be associated with the stability of the device and could disturb the evaluation of passivation process. Hydrogen is a well-known extrinsic impurity that forms shallow donor states in ZnO-based semiconductors. The application of $SiN_x$, as the first passivation layer converts GIZO into a simple resistor. This results from the incorporation of hydrogen during the plasma-enhanced chemical vapor deposition of $SiN_x$, which uses a mixture of silane ($SiH_4$) and ammonia ($NH_3$) precursors. These can induce very large concentrations of hydrogen in the plasma, and hydrogen radicals prefer oxide semiconductors conductive. Therefore, chemical vapor deposited SiO$_x$ (2000A) films were deposited at fixed process conditions as the first protective layer in all devices to suppress the hydrogen contamination of GIZO and obtain the reasonable initial characteristics of the device even though this layer could affect the stability of the device.

The typical responses of the oxide TFT transfer curves to the
NBITS conditions are shown in Fig. 1a. During the NBITS, the only affected parameter was the threshold voltage ($V_{th}$) of the transistor. Other TFT parameters including on/off current levels and the slope of the transfer curves were not changed after the stress.

In addition, the $V_{th}$ values of the curves were recovered from the shifted values after some hours passed when they were laid under no stress condition. The initial values of $V_{th}$ are recoverable by leaving the devices untested in the dark after some hours.

The $V_{th}$ shift was attributed to the charge trapping at the shallow traps, which can be easily recovered by a small amount of the external energy.

The measured $V_{th}$ shifts of the GIZO TFTs with different types of passivation structures under NBITS in humid ambient are depicted in Fig. 2a. Devices I and II exhibit similar amounts of $V_{th}$ shifts for the first 3 h. A considerable difference was then observed at longer stress times. The stability of device II, which has an additional SiN$_x$ layer on top, is superior to that of device I that has only a single SiO$_x$ passivation. The $V_{th}$ shift of device II is about $\sim$3.2 V, but device I undergoes a larger shift of $\sim$5.7 V. Device III, of which the passivation layer is composed of high temperature SiO$_x$ and SiN$_x$, exhibits the smallest amount of $V_{th}$ shift among the three types of TFTs.

Figure 2b shows the amount of threshold voltage shift of each type of TFT with respect to logarithmic time. Fitting lines are shown on the plots to estimate the rates of $V_{th}$ shift. An abrupt increase in the shift rate is observed for device I after 3 h of stress. This suggests that there may be two different mechanisms that govern the threshold voltage shift in the short and long stress time regions.

Unlike device I, device II shows an almost constant $V_{th}$ shift rate under NBITS. This implies that the existence of the topmost SiN$_x$ promotes better device stability even for extended NBITS durations. At this point, the additional SiN$_x$ layer effectively impedes the indiffusion of external molecules down to GIZO and results in a relatively smaller $V_{th}$ shift compared to a TFT with a single SiO$_x$ passivation. Silicon nitride is reported to be a better diffusion barrier than SiO$_x$. Here, the time evolution of $V_{th}$ for device I suggests that the moisture from the humid ambient readily diffuses across the silicon oxide layer during the short bias period and as it contaminates the GIZO surface, an abrupt acceleration in $\Delta V_{th}$ begins to take place (longer stress time). The microstructure of the SiO$_x$ films was examined by transmission electron microscopy (TEM) (Fig. 3).

The layer deposited at 150°C contains relatively large concentrations of nanometer-scale voids, uniformly distributed over the film’s thickness and area. The external humidity and other gas molecules can thus permeate through these empty regions. Moisture reaching the GIZO film enhances the generation of shallow donor states created by visible light radiation and induces an increase in carrier density within GIZO. Such a phenomenon makes the n-type metal-oxide-semiconductor device operate closer to the depletion mode and so shifts the threshold voltage toward negative values. Here, it can be deduced that the abrupt acceleration of $\Delta V_{th}$ in device I (Fig. 2b) results from the above mechanism.

To examine the effect of the adsorption of water molecule from the environment, the value of $V_{th}$ of device I under the vacuum NBITS stress condition was recorded; the value of $V_{th}$ reached up to approximately $\sim$2.0 V and remained at almost a constant value after 30 min. This agrees well with our proposed models in which the external water permeating through the passivation layers plays an important role in the long period stability of the oxide TFT device.

A significant difference in the behavior of $V_{th}$ is observed between devices II and III throughout the entire NBITS duration. Such a disparity suggests that the deposition temperature of SiO$_x$ directly in contact with the GIZO layer has a strong influence on device reliability. The difference in the amount of the $V_{th}$ shift seems to originate from the difference in bond structure at the GIZO/SiO$_x$ interface bonding state. The silicon oxide layer in device III was deposited at a higher temperature so that much stronger bonds could be formed at the interface. Device I, where the silicon oxide layer was deposited under the same conditions as in type II, shows similar behavior in the short time region. The quality of the GIZO/SiO$_x$ interface is conjectured to determine the $V_{th}$ shift of all TFTs in the initial region of the NBITS tests.

It has been reported that UV light radiation on oxide semiconductor TFTs results in negative threshold voltage shifts due to the generation of oxygen vacancies, which are also known as shallow donors. The wavelength of the halogen lamp used in the present NBITS experiments lies within the visible range of the spectrum. Thus, the photon energies are not sufficiently high to generate large amounts of oxygen vacancies in the GIZO films. However, weak GIZO/SiO$_x$ interface bonds are believed to act as hole traps generated by the photon energy of visible light. These defects release electrons by trapping holes from the GIZO bulk and as a result
Induce negative $V_{th}$ shifts as if n-type doping occurred. Consequently, the small threshold voltage shift observed in device III over the entire NBITS period is attributed not only to the presence of the less permeable silicon nitride layer but also to the highly compact SiO$_x$ structure and stable interface that it forms with the underlying GIZO.

In summary, three types of GIZO TFTs with different passivation structures were fabricated and subjected to NBITS in a humid environment. The GIZO TFTs exhibit different NBITS behaviors depending on their passivation conditions. GIZO TFTs with double layer passivation stacks undergo smaller negative $V_{th}$ shifts. In the short stress time region, the amount of threshold voltage shift seems to be related to the quality of the GIZO/passivation interface. The number of defects at the GIZO/passivation interface appears to be significantly reduced by increasing the deposition temperature. In the long stress time period, the threshold voltage shift depends on the ability of the passivation system to impede the diffusion of external moisture. The additional silicon nitride grown onto the first silicon oxide protective layer effectively suppresses such a detriment. From the TEM observation at high magnifications, high densities of pores were present in the silicon oxide film grown at a relatively low temperature and these seem to provide fast diffusion paths to the external moisture, which reach the GIZO surface and thereby generate shallow donor states. This is associated with the rapid increase in the threshold voltage shift at longer NBITS times for device I.

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