The Effect of Dynamic Bias Stress on the Photon-Enhanced Threshold Voltage Instability of Amorphous HfInZnO Thin-Film Transistors

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Abstract—The electrical stability of amorphous HfInZnO (HIZO) thin-film transistors (TFTs) was investigated under static and dynamic stress conditions, with simultaneous visible light radiation. The extent of device degradation is found to be strongly sensitive to the gate voltage, pulse duty ratio, pulse frequency, and exposure to visible light. Dynamic stress experiments demonstrate that highly stable devices can be realized by adjusting the pulse duty ratio and frequency, which suggests that amorphous HIZO TFTs are a promising candidate of switching devices for large-area high-resolution AMLCD applications.

Index Terms—Dynamic stress, HfInZnO, instability, thin-film transistor (TFT).

I. INTRODUCTION

RECENTLY, thin-film transistors (TFTs) employing amorphous oxide semiconductors such as Ga–In–Zn–O (GIZO) and Hf-In-Zn-O (HIZO) have been subject of intensive study as promising alternatives to a-Si devices, owing to their high field-effect mobility (> 10 cm²/Vs), excellent subthreshold swing (< 0.4 V/decade), and high \( I_{ON}/I_{OFF} \) ratios (> 10⁷), which are superior to those of their a-Si counterparts [1]–[5].

In an operating AMLCD device, the switching transistor that experiences a continuous pulsed gate voltage is inevitably exposed to light, due to the presence of the back light unit underneath. However, most of the reports available in the literature involve the bias stress-induced instability of oxide TFTs with static bias stress only or in the dark [6]–[9]. The examination of bias stress instability under dynamic stress with backlight illumination mimics real operating conditions and allows a more reasonable approximation of the reliability of oxide TFTs for AMLCD backplanes.

In this letter, the effects of static and dynamic stresses on the photon-enhanced threshold voltage instability of HIZO TFTs are observed, which have recently been developed and shown to exhibit excellent electrical performance [5].

II. EXPERIMENTAL PROCEDURE

A bottom gate HIZO TFT was fabricated, as shown in Fig. 1, which is similar to that of conventional a-Si TFTs. The detailed fabrication process is described in a former report [1]. A SiNₓ (400 nm) gate dielectric layer was deposited using plasma-enhanced chemical vapor deposition (PECVD) with a substrate temperature of 350 °C. A HIZO film (70 nm) was then grown as the active channel layer using RF magnetron sputtering at room temperature with a single ceramic target (\( \text{HfO}_2 : \text{In}_2\text{O}_3 : \text{ZnO} = 0.19:1:2 \text{ mol} \)). After patterning the source and drain electrodes, a SiOₓ passivation layer with a thickness of 200 nm was deposited by PECVD at 150 °C. The resulting device was then annealed in air at 250 °C for 1 h. The device characterization was carried out using a Keithley 4200 semiconductor parameter analyzer, which consists of a heating stage, a light generator, and an electrical pulse generator. During the illumination stress test, the devices were exposed to white light emanating from the BLU, with a brightness of 20000 cd/m². All measurements were performed on TFTs with channel width/length = 90/8 μm.

III. RESULTS AND DISCUSSIONS

We first describe the impact of photon radiation on the instability of HIZO TFTs under static stress. Fig. 2(a) and (b) shows the evolution of transfer curves as a function of the applied negative bias temperature stress (NBTS) time in dark and under illumination, respectively. During stress periods, \( V_{GS} \) and \( V_{DS} \) were fixed at −20 and +10 V, respectively, and a stage temperature of 60 °C was maintained. For bias stress tests with light illumination, the backlight is turned on during the sampling periods as well as the stress periods. The field-effect...
mobility ($\mu_{FE}$) in the saturation regime was extracted from $I_{DS}$–$V_{GS}$ characteristics, in compliance with the gradual channel approximation [2]. We define the threshold voltage ($V_T$) as the $V_{GS}$ that induces a drain current ($I_{DS}$) of 1 nA, which is an important parameter regarding switching TFTs.

A pristine device measured in the dark [Fig. 2(a)] exhibits a $\mu_{FE}$ value of 2.4 cm$^2$/V-s, SS value of 0.3 V/decade, and $V_T$ of $-0.23$ V. The $V_T$ slightly moves to $-1.42$ V after 3 h of stress. On the other hand, the NBITS experiments with BL illumination [Fig. 2(b)] result in a much larger negative $V_T$ shift of $-10.9$ V after 3 h of stress. It is also noted that the large negative shift of $V_T$ under NBITS conditions does not involve any change in $\mu_{FE}$ or SS with respect to stress time.

Fig. 2(c) shows the magnitudes of $V_T$ shift ($|\Delta V_T|$) as a function of the applied positive bias temperature stress (PBTS) and NBTS time with and without BL illumination. For PBTS experiments, the applied $V_{GS}$ was set to $+20$ V while keeping other variables such as $V_{DS}$ and substrate temperature identical to those used in NBTS studies. In Fig. 2(c), the direction of $V_T$ shift for NBTS and PBTS is negative and positive, respectively, regardless of light illumination. It is noted that the BL illumination has a more pronounced influence on $I_{DS}$–$V_{GS}$ characteristics, in compliance with the gradual channel approximation [2]. We define the threshold voltage ($V_T$) as the $V_{GS}$ that induces a drain current ($I_{DS}$) of 1 nA, which is an important parameter regarding switching TFTs.

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The stretched exponential equation, which is defined as

$$I(t) = I(0) \exp \left[ -\left( \frac{t}{\tau} \right)^\beta \right]$$

where $I(0)$ is the initial current, $\tau$ represents the characteristic time constant, and $\beta$ is the stretched exponential exponent [7]. The stretched exponential parameters for each stress condition are listed in Table I. The stretched exponential time dependence and negligible changes of SS suggest that charge trapping in the gate dielectric bulk or at the gate dielectric/channel interface is the dominant mechanism for $V_T$ instability of HIZO TFTs. The BL illumination accelerates the negative $V_T$ shift, by providing excess photo-generated holes, which become trapped under negative bias stress [10].

Next, the effects of dynamic stress on the photon-enhanced $V_T$ instability of HIZO TFTs are examined. A rectangular wave was used as the source of dynamic pulse, as shown in the inset of Fig. 3(a). The duty ratio ($D$) is given by the ratio of $t_{ON}$ to pulse period ($T$). The $V_{ON}$ and $V_{OFF}$ were fixed to $+20$ V and $-20$ V, respectively. Fig. 3(a) and (b) shows the duty ratio dependence of $V_T$ shift after 3 h in low duty ratio and high duty ratio region, respectively. The frequency was fixed at 60 Hz.

The frequency dependence of $\Delta V_T$ and estimated $\Delta V_T$, using the stretched exponential equations obtained from dc stress tests, respectively. Negative shifts in $V_T$ were observed in the low duty ratio region ($\leq 1\%$), while positive $\Delta V_T$ values were obtained with high duty ratios ($\geq 10\%$). One may anticipate negative $V_T$ shifts in the low duty ratio region, where the “off” state is dominant. However, it should be noted that negative $V_T$ shifts are considerably reduced by the addition of a short “on” pulse. $\Delta V_T$ was then calculated as the sum of

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>STRETCHED EXPONENTIAL PARAMETERS UNDER VARIOUS STRESS CONDITIONS</th>
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<tr>
<td>$\tau$ (s)</td>
<td>$\beta$</td>
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<tr>
<td>PBITS</td>
<td>1.6E+09</td>
</tr>
<tr>
<td>NBITS</td>
<td>2.8E+05</td>
</tr>
<tr>
<td>NBTS</td>
<td>1.3E+11</td>
</tr>
<tr>
<td>NBITS</td>
<td>2.0E+04</td>
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Fig. 3. Duty ratio dependence of $\Delta V_T$ at a frequency of 60 Hz in (a) low duty ratio ($\leq 1\%$) region and (b) high duty ratio ($\geq 10\%$) region. (Inset) Applied ac square wave pulse. (c) Frequency dependence of $\Delta V_T$ at a duty ratio of 0.1%.
the $V_T$ shift for the total duration of negative and positive bias stresses, using the stretched exponential equation weighed by each portion of positive and negative dc stress

$$
\Delta V_T = \Delta V_{TP} + \Delta V_{TN}
= \Delta V_{TP}(0) \left\{ 1 - \exp \left[ -\left( DT_{ST}/\tau_{TP}\right)^{\beta_p} \right] \right\} \\
+ \Delta V_{TN}(0) \left\{ 1 - \exp \left[ -\left( (1 - D)T_{ST}/\tau_{TN}\right)^{\beta_n} \right] \right\}.
$$

In Fig. 3(a), as the duty ratio increases, larger differences between the measured and the estimated values for $\Delta V_T$ are observed. This phenomenon may be interpreted as follows. During the “on” pulse, the already trapped holes become detrapped and annihilated through the recombination process with electrons. From the equation of $\Delta V_T = \Delta N_{eff}/C_I$, the number of trapped hole under dc stress and dynamic stress with 1% duty can be estimated to $7.60 \times 10^{11}$ cm$^{-2}$ and $1.01 \times 10^{11}$ cm$^{-2}$, respectively, suggesting that 87% of photo-generated holes are annihilated. Since the trapping rate is proportional to the existing charge concentration, the reduction of hole concentration in the “ON” state induces a net decrease in negative $V_T$ shift. Therefore, under dynamic stress with the presence of light, the reduction of negative $V_T$ shift can be attributed to the detrapping and successive extinction of photo-generated holes.

On the other hand, in the high duty ratio region, complete annihilation of the photo-generated holes occurs, and so, the threshold voltage shift is mainly associated with electron trapping during the “ON” state. From Fig. 3(b), positive shifts in $V_T$ are observed, and the measurement data fit well with the estimated values, based only on the stretched exponential equation for the positive bias stress and time.

Fig. 3(c) shows the frequency dependence of $V_T$ shift with a duty ratio of 0.1%. The magnitude of $\Delta V_T$ decreases with increasing frequency. This behavior can also be interpreted by the recombination process. As the pulse frequency increases, the number of positive pulse per unit time increases. Once a positive pulse is applied, the hole trapping rate during the subsequent negative pulse should continuously decrease owing to the reduction of hole concentration.

IV. Conclusion

In this letter, the photon-enhanced threshold voltage instability of amorphous HIZO TFTs under both static and dynamic stresses has been evaluated. Compared to static stress conditions, superior electrical stability under dynamic stress even with BL illumination has been observed particularly at higher pulse frequencies. The aforementioned results have suggested that by properly optimizing the pulse conditions, the operating lifetime of oxide semiconductor TFTs can be prolonged and so will allow the realization of large-size and high-resolution AMLCD products.

REFERENCES