Recent progress in high performance and reliable n-type transition metal oxide-based thin film transistors

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Invited Review

Recent progress in high performance and reliable n-type transition metal oxide-based thin film transistors

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Abstract
This review gives an overview of the recent progress in vacuum-based n-type transition metal oxide (TMO) thin film transistors (TFTs). Several excellent review papers regarding metal oxide TFTs in terms of fundamental electron structure, device process and reliability have been published. In particular, the required field-effect mobility of TMO TFTs has been increasing rapidly to meet the demands of the ultra-high-resolution, large panel size and three dimensional visual effects as a megatrend of flat panel displays, such as liquid crystal displays, organic light emitting diodes and flexible displays. In this regard, the effects of the TMO composition on the performance of the resulting oxide TFTs has been reviewed, and classified into binary, ternary and quaternary composition systems. In addition, the new strategic approaches including zinc oxynitride materials, double channel structures, and composite structures have been proposed recently, and were not covered in detail in previous review papers. Special attention is given to the advanced device architecture of TMO TFTs, such as back-channel-etch and self-aligned coplanar structure, which is a key technology because of their advantages including low cost fabrication, high driving speed and unwanted visual artifact-free high quality imaging. The integration process and related issues, such as etching, post treatment, low ohmic contact and Cu interconnection, required for realizing these advanced architectures are also discussed.

Keywords: field-effect transistors, metal oxide, high performance

(Some figures may appear in colour only in the online journal)

1. Introduction

Transition metal oxide (TMO) semiconductors with n-type conductivity have attracted enormous attention as a channel layer of pixel switching transistors in the area of active matrix devices, such as liquid crystal displays (LCDs) and organic light-emitting diodes (OLEDs), because they offer intriguing properties, such as high mobility, good transparency to visible light, low temperature process capability and relatively low fabrication cost compared to silicon-based semiconductors [1, 2]. In particular, the conduction band of TMO materials is associated with overlap of the ns orbitals of transition cations, such as zinc, indium and tin. Their non-directionality allows disordering-independent carrier mobility, low trap state density and good uniformity of the resulting TMO TFTs [3, 4]. The applications of flat-panel AM displays include mobile telephones, tablets, monitors, and televisions according to the panel size. Traditional amorphous Si (a-Si) and low temperature polycrystalline silicon (LPTS) backplanes are still the mainstream for such products. In the case of mobile telephones, the LPTS thin film transistors (TFTs) array is rapidly penetrating the high-end LCD and OLED products because...
they exhibit very high mobility (>80 cm²Vs⁻¹), excellent electrical stability and good form factor. On the other hand, televisions, which have the largest market volume among the various applications, is driven by a-Si TFT arrays. This is due to the large size uniformity, scalability and low fabrication cost of a-Si backplane technology [5, 6]. The application of TMO electronics to practical products depends on the design specifications of each panel. For mobile applications, TMO TFTs with high mobility compatible to the LTPS counterpart need to be developed. Considering that the typical mobility of In₂Ga₂ZnO₇ TFTs is approximately 10 cm²Vs⁻¹ in the manufacturing line, it is imperative to develop an advanced composition and device structure of TMO TFTs with high field-effect mobility (>30 cm²Vs⁻¹), as shown in figure 1. Although higher mobility (>20 cm²Vs⁻¹) can be achieved for In-rich IGZO films [7–9], the reliable and production grade composition of the IGZO channel layer for TFTs is limited in the flat panel display industry. For the large size television applications, the most important aspect is the low fabrication cost. TMO TFTs can be fabricated without an intentional crystallization and ion doping process, which are essential processes for LPTS TFTs. Therefore, TMO TFTs are potentially attractive for low cost fabrication. The overall panel cost of flat panels is determined by the architecture of the TFTs, which can be classified as a bottom gate, top gate or coplanar structure. The most popular architecture of a-Si TFTs is a bottom gate structure (figures 2(a) and (b)), where the source/drain electrode is formed on the semiconducting layer. In particular, the back-channel-etch (BCE) type is preferred due to the simplicity of the process and the lowest use of photomask steps (figure 2(b)). On the other hand, TMO TFTs, which have been studied thus far, are the etch stopper (ES) type because the TMO channel is attacked easily by S/D patterning damage (figure 2(a)). Therefore, the development of TMO TFTs with a BCE type is essential for reducing the fabrication cost.

High resolution (≥200 ppi) and high frequency frame (≥240 Hz) driving have become a megatrend for the next generation active-matrix (AM) displays, which enable a vivid image and a natural motion picture in the resulting display. On the other hand, these requirements shorten the scan line selection time, leading to insufficient charging (image error) in the storage capacitor of each pixel. To resolve this problem,
extensive efforts are needed including high mobility, low resistance and low capacitance with the aim to reduce the resistive-capacitive (RC) delay (figure 1). In addition, undesirable visual artifacts, such as flicker and image sticking, etc, can be aggravated by the displacement current caused by parasitic capacitive coupling. In particular, the kick-back effect due to the parasitic capacitance of TFTs is the origin for the flicker and image sticking problem in AMLCD and AMOLED panels, respectively [10]. Therefore, the design and fabrication of TFT arrays with a low parasitic capacitance, such as a self-aligned coplanar structure, is also a technically important issue (figure 2(c)).

Several excellent review papers on TMO TFTs in terms of the fundamental electron structure, device process and reliability have been published [11–14]. In this review, the novel channel composition and channel structure reported recently focused on the In-Zn-Sn-O (IZTO), zinc oxynitride (ZnON) semiconductor, double channel and hybrid composite channel. The sputtering technique is the most commonly used method for preparing TMO films because of its higher performance and superior electrical or photo stability compared to the counterpart of the solution-based processing. Kim et al recently reviewed solution processed TMO and related devices, which have the advantages of a simple process, low cost and high throughput [15]. Beside the traditional ES type device, BCE type TMO TFTs with the merit of process simplicity and short channel device are also addressed in terms of the etching, treatment, passivation and copper (Cu) line processes. Finally, the fabrication process and issues of TMO TFTs with a self-aligned coplanar structure are reviewed, which enables realization of a visual artifact-free image in the resulting AM displays.

2. Compositional approach for high performance TFT

2.1. Binary TMO semiconductor

Binary oxides, such as ZnO, In₂O₃ and SnO₂, have a wide band gap (>3.0 eV) and high electrical conductivity, which can be attributed to native defects, such as oxygen vacancies, cation interstitials, hydrogen, which act as shallow donors [16–18]. These oxides have high electron mobility even when they are amorphous, which originates from the intercalation of the ns orbital of the cations [19, 20]. For these reasons, these oxides have been considered widely as the base materials for amorphous semiconductors. Since the first report of ZnO TFTs by Hoffman et al [21], the performance of ZnO TFTs have been improved steadily by optimizing the sputtering process or solution process [22–25]. Recently, modification of the device structure, such as the vertical channel [26] and dual gate [27], has been also reported using a ZnO semiconductor. On the other hand, ZnO is a polycrystalline material that is unsuitable as a channel material for TFTs because of its non-uniformity [1, 17, 28]. Therefore, the key issue for ZnO semiconductors is to obtain grain boundary-free uniform properties, which should not be compromised by any degradation of the high electron mobility, via a simple process. The extraordinary mobility of ~120 cm² Vs⁻¹ was previously reported for InO TFTs with an organic dielectric. Despite this, these devices suffer from a large off-state current and low On/Off ratio of ~10⁵ presumably due to the high leakage current of the organic dielectric and/or the high conductivity of the InO, channel layer itself [29].

2.2. Ternary TMO semiconductor

With the viewpoint of large area uniformity, the ternary TMO semiconductor would be promising because a multi-component cation system is immune to crystallization under a given processing condition. InZnO (IZO) is the representative ternary system. In₂O₃ and ZnO have the bixbite and wurtzite crystal structure, respectively. Owing to the different geometrical hindrances, the two components have also different cation coordination numbers, which allow the resulting IZO alloy to be an amorphous phase. In addition, the resistivity of IZO films varies dynamically from 10⁻⁴ to 10⁸ Ωcm by controlling the cation composition and cation/oxygen non-stoichiometry. This means that the IZO film can be used as either a transparent conducting electrode or channel layer of TFTs for FPD application [30–33]. On the other hand, the IZO film exhibits a high free electron density (Nₑ) because of the easy formation of oxygen vacancy defects, which deteriorates the off-state current and photobias stability of the resulting IZO TFTs. For example, a high mobility of >100 cm² Vs⁻¹ was reported for the IZO TFTs with a good Iₘ₉/Iₒ₉ Ratio of 10⁵ [34], but the NBIS stability of the IZO TFTs was not studied. Recently, IZO TFTs with high mobility (>30 cm² Vs⁻¹) have been reported (figure 3), where the photobias stability was reinforced by oxygen high pressure annealing [35].

ZnSnO (ZTO) is another ternary class material that easily forms an amorphous phase. In contrast, the ZTO system is
much cheaper than the IZO system. Therefore, there have been many reports regarding the promising performance of TFTs with a ZTO channel layer [36–43]. The stability of ZTO TFTs was improved by either optimizing the Zn/Sn ratio [38] or controlling the passivation process [41]. On the other hand, it is difficult to pattern tin-rich ZTO by wet etching. Moreover, the device instability of ZTO TFTs under bias thermal stress (BTS), light illumination or negative bias illumination stress (NBIS) conditions require further improvement.

2.3. Quaternary TMO semiconductor

A low $N_c (<10^{17} \text{cm}^{-3})$ is a key technical parameter for achieving highly stable TMO TFTs. In the case of binary or ternary TMO systems, moderate n-type doping can be controlled by the cation/anion non-stoichiometry or process optimization. An alternative approach is to introduce an extra component, which is called a carrier suppressor. Gallium (Ga) is a representative carrier suppressor for the IZO system. Nomura et al reported high performance TFTs with an IGZO channel, where $N_c$ was reduced by the Ga fraction [1]. This reduction of $N_c$ can be explained by the high ionic field strength of the Ga ion, which allows oxygen to be bound tightly and prevents the formation of oxygen vacancies [1, 20, 28, 44]. In the IGZO TFTs, the carrier mobility generally increased with increasing In content (decreasing Ga content), which can be explained by the increasing $N_c$. Therefore, high mobility ($>20 \text{cm}^2 \text{Vs}^{-1}$) can be achieved for TFTs with an In-rich IGZO channel composition [7–9]. Many other carrier suppressors, which are similar to the Ga ion, have been suggested for IZO and ZTO. Hafnium (Hf) was proposed as an effective carrier suppressor for the IZO semiconductor [45]. The fabricated HIZO TFTs exhibited reasonable device performance with a field-effect mobility of $\sim 10 \text{cm}^2 \text{Vs}^{-1}$, and high $I_{on/off}$ ratio of $>10^4$. The photobias stability of the HIZO TFTs was improved further by either choosing a SiO$_2$ dielectric as a gate insulator [46] or adopting a double etch stop layer [47]. Park et al reported highly stable Zr-doped IZO (IZIZO) TFTs, where the ZrO$_2$ was introduced as a carrier suppressor [48]. The $N_c$ in the ZIZO films decreased from $4 \times 10^{16} \text{cm}^{-3}$ to $1 \times 10^{14} \text{cm}^{-3}$ with increasing Zr fraction. The ZIZO TFTs annealed at 350 °C for 2 h. exhibited a field-effect mobility of 3.9 cm$^2$Vs$^{-1}$, $\mu$ factor of 0.98 V/decade, $V_{th}$ of 1.6 V, and an $I_{on}/I_{off}$ ratio of $\sim 10^7$. The constant current stress ($I_{DS} = 3 \mu\text{A}$, $V_{DS} = 10 \text{V}$, 60 h.) stability ($\Delta V_{th} = 1.0 \text{V}$) of the ZIZO TFTs was superior to that ($\Delta V_{th} = 3.4 \text{V}$) of IGZO TFTs. Titanium [49, 50], aluminium [51, 52], tantalum [53], strontium [54], barium [54], scandium [55], magnesium [56], lanthanum [57], and gadolinium [58] exhibit similar carrier suppressor behavior in the IZO-based system, as shown in figure 4.

One promising composition toward high mobility in quaternary TMO materials is the IZTO semiconductor [60]. High temperature annealing under an oxidizing atmosphere favors the Sn$^{2+}$ to Sn$^{4+}$ transition in the TMO film. Figures 5(a) and (b) shows the transfer characteristics and mobility variations of the representative IZTO TFTs with the atomic ratio of In:Zn:Sn = 40:36:24. A high mobility of $52.4 \text{cm}^2 \text{Vs}^{-1}$ and low $\mu$SS factor of 0.2 V/decade were observed without a deterioration of the off-state drain current and $V_{th}$ value ($I_{on/off}$ ratio $>2 \times 10^8$, $V_{th} \sim 0.1 \text{V}$) [61]. On the other hand, the introduction of a carrier suppressor in the IZO system tended to reduce the mobility of the TFTs (so called percolation conduction), even though it improved substantially the resistance of the TFTs against an external gate bias stress and photobias stability. The strong trade-off between the mobility and stability of TMO TFTs will be described in the next section.

2.4. Oxynitride semiconductor

The cation composition has been modified mainly to improve the stability of TMO TFTs under bias and illumination stress. An entirely different approach was proposed using ZnON as a channel layer [62, 63]. The substitution of an oxygen anion with a nitrogen anion in ZnO reduces the energy band gap of ZnON to 1.3 eV, which eliminates the oxygen deficient-
related deep levels near the valence band maximum. Therefore, the photobias stability of the resulting ZnON TFTs becomes comparable to that of the LTPS TFTs (figure 6) [63]. Simultaneously, a high mobility of >40 cm²Vs⁻¹ can be achieved due to the effective small electron mass in ZnON films. On the other hand, the severe stretch-out of the sub-threshold drain current suggests the existence of huge tailing trap states that need to be resolved.

3. Advanced architecture for high performance TFTs

3.1. Double channel structure

In a-IGZO system, the wave function of the ns orbital of In³⁺ overlaps first and forms delocalized states in the conduction band because the indium ion has the largest ionic size among the various cations. The increasing In content in the a-IGZO
film gives rise to a simultaneous increase in Hall mobility and \( N_e \), which can be explained by the formation of shallow oxygen vacancies that is facilitated by increasing the coordination number of In ions around a given oxygen atom. In particular, the proportional relationship between the carrier density and mobility can be understood by a so-called percolation conduction mechanism. This means that the enhancement in the field-effect mobility by increasing In content normally accompanies the serious degradation in both off-state drain current and \( I_{on}/I_{off} \) ratio in the IGZO TFTs. This tradeoff relation limits the use of the \( I_{on} \) fraction to achieve high mobility. The photo bias stability of metal oxide TFTs can also be aggravated seriously by the increasing In fraction. Most oxygen vacancies except for a few oxygen vacancy species were calculated to be an inactive and deep state in the forbidden energy gap of IGZO materials [2]. The exposure of photons (>2.2 eV) on the IGZO material causes the phot ionization of neutral oxygen vacancies \( (V_O) \) to meta-stable positively-charged oxygen vacancies \( (V_O^{2+}) \). During the phot ionization process, the two electrons \( (V_O \rightarrow V_O^{2+} + 2e^-) \) released gives rise to photon-induced electron doping, which results in a negative shift of \( V_{th} \) in the IGZO TFTs [11]. Therefore, achieving a high field-effect mobility without the degradation of photobias stability is a challenge. As an alternative approach, the double-channel structure can provide a solution to the adverse tradeoff between the field-effect mobility and photo-bias stability [64–68].

All double-channel devices studied had a bottom gate and top contact configuration. The channel layer consisted of a front layer and back layer. The front channel layer inserted between the gate dielectric film and back channel layer plays the role of the mobility booster, whereas the back channel layer strengthens the resistance of the TFTs to external gate bias and light stress. Therefore, the physical thickness \( (t_{int}) \) and \( N_e \) of the interfacial front layer is a critical factor for determining the overall device performance of the double channel TFTs. A reasonable window for the interfacial layer in terms of the \( t_{int} \) and \( N_e \) values can be expected, which does not cause any degradation of the \( V_{th} \) and \( I_{off} \) parameters. Given that the \( N_e \) of the interfacial channel layer is much larger than that of the back channel layer, it can be assumed that the \( V_{th} \) and \( I_{off} \) values for the double channel TFTs are determined by the conducting front layer. First, to sustain the low \( I_{off} \) value, the \( t_{int} \) value should be smaller than the depletion thickness \( (x_{dep}) = (2\varepsilon_0 K_s/\varepsilon q N_e)^{1/2} \), where \( \varepsilon_0 \) is the vacuum permittivity, \( K_s \) is the relative dielectric constant of a semiconductor, \( \phi_e \) is the channel surface bending and \( q \) is the elementary charge, which corresponds to guide line (i) in figure 7. Second, the total number \( (q t_{int} N_e) \) of free electrons in the channel must be less than the number of charge carriers \( (Q_G) \) induced by the gate dielectric capacitor \( (Q_G = C_G V_{GS} = \varepsilon_0 K_G V_{GS}/\varepsilon_G) \), where \( K_s \) is the relative dielectric constant of the gate insulator, and \( \varepsilon_G \) is the gate insulator thickness), which determines guide line (ii). The \( t_{int} \)-dependent \( N_e \) values should belong to the shaded area for the suitable operation of transistors. Otherwise, the device would suffer from either a large negative \( V_{th} \) value and/or a large \( I_{off} \) current. Kim et al reported high performance TFTs with a double-channel structure consisting of a thick back IGZO and thin front IZO (or ITO) layer, as shown in figure 8 [64]. TFTs with a single 70 nm thick IGZO channel exhibited a moderate mobility of 19.2 cm² Vs⁻¹. \( V_{th} \) of -0.6 V and an \( I_{off} \) value of 5.7 × 10⁻¹³ A. A substantially higher mobility of 55.2 cm² Vs⁻¹ was obtained for TFTs with a single 30 nm thick IZO channel layer. The \( V_{th} \) value of the IGZO TFTs, however, degraded to -8.2 V. The improved mobility and degraded \( V_{th} \) value of the IZO TFTs was attributed to the high \( N_e \) of the IZO channel layer, even though the actual \( N_e \) values of the IZO films were not characterized. In contrast, the double channel TFTs with a back IGZO(70 nm)/front IZO (5 nm) showed a high mobility of 51.3 cm² Vs⁻¹ and a low \( I_{off} \) of 4.7 × 10⁻¹³ A without sacrificing the \( V_{th} \) value (-0.3 V).
This suggests that the conducting interfacial IZO or ITO between IGZO and the SiO₂ film induces the high mobility of the resulting TFTs. The thickness of the conducting IZO or ITO layer should be controlled carefully because the thick IZO or ITO layer (>8 nm) in the double channel TFTs can cause a huge negative $V_{th}$ value [64]. The concept of a conducting channel path as an enabler of high mobility was confirmed in the IGZO TFTs with a buried channel of the GZO film [65]. The insertion of a conducting GZO film with a carrier density of $3.9 \times 10^{19}$ cm$^{-3}$ between the semiconducting IGZO and SiO₂ dielectric film allowed enhanced mobility and better positive bias stress (PBS) stability of the resulting TFTs compared to those of the TFTs with a single IGZO channel. The result of a device simulation indicated that the screening length of the buried channel device was smaller than that of the single IGZO device when the positive gate voltage was applied. The insensitive surface potential variation near the channel region of the buried channel device resulted in less trapping of the charge carriers, which allowed better PBS stability of the resulting TFTs.

The thickness effect of the thin front ITO film on the transporting property and PBS/negative gate bias stress (NBS) induced instability in the double-channel Zn$_{0.7}$Sn$_{0.3}$O (ZTO)/In$_{0.9}$Sn$_{0.1}$O(ITO) TFTs was investigated in detail. The PBS and NBS stability as well as the mobility of the ZTO/ITO TFTs were improved with increasing $t_{int}$ (≤3.5 nm) compared to those of the single channel ZTO device, which was attributed to a decrease in the effective interfacial trap density. The ZTO/ITO(4.5 nm) TFTs, however, suffered from inferior NBS stability to that of single channel ZTO TFTs, whereas their mobility was enhanced further to 45.0 cm$^2$ V$^{-1}$s$^{-1}$ [67]. The density-of-state (DOS)-based design concept was proposed for the double-channel TMO TFTs. The DOS-based optimized Hf$_{0.10}$In$_{0.35}$Zn$_{0.55}$O(HIZO)/In$_{0.85}$Zn$_{0.15}$O(IZO) TFTs exhibited superior BOTS stability as well as a higher mobility of 48.0 cm$^2$ V$^{-1}$s$^{-1}$ compared to those of the single channel HIZO or IZO TFTs [68]. On the other hand, the fundamental and puzzling question is why the optimal front channel thickness ($t_{int}$) for high performance TFTs without an accompanying deterioration of the BTS stability was

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**Figure 9.** (a) Change in $V_{th}$ for various double channel ZTO/IZO devices with a different $t_{int}$. The empty and filled symbols denote the PBS and NBS induced variations, respectively. (b) Calculated density-of-states distribution as a function of ($E-E_C$) for the devices examined. (c) Amorphous structure of ITZO, including eight formula units of In$_2$Zn$_2$Sn$_2$O$_9$ and the calculated formation energies of VO as a function of the number of neighboring Sn atoms. Reproduced with permission from [69].
ordered a high mobility of 79.0 cm²Vs⁻¹ channel layer. This NDD on the IGZO channel region rendered a porous gate mask to increase the conductivity of the IGZO channel allowed a porous gate structure, which was used for polystyrene sphere and subsequent etching of the IGZO performance of the ZnO/Al₂O₃ superlattice TFTs was attributed to the NDD-induced barrier lowering of the channel layer and thus the carrier mobility of the In₀.₅₀Zn₀.₅₀O/single-walled carbon nanotube (SWNT) was channel structure consisting of sol-gel processed film consisting of a ZnO/Al₂O₃ stack was reported to exhibit better transporting and gate bias stress stability than those with a single ZnO channel, as shown in figure 10. The superior performance of the ZnO/Al₂O₃ superlattice TFTs was attributed to the quantum confinement effect, improved crystallinity of the ZnO channel and passivation effect of the Al₂O₃ film.

The electrical properties of the TMO semiconductor can be tailored by adopting a composite structure. The hybrid channel structure consisting of sol-gel processed In₀.₅₀Zn₀.₅₀O/single-walled carbon nanotube (SWNT) was used to produce high performance, flexible TFTs. This composite channel device exhibited a high mobility of 140 cm²Vs⁻¹, whereas a high \(\mu_{\text{on/off}}\) ratio of \(~10^7\) was maintained [72]. The reason for the high mobility is that the SWNTs in a composite channel provide a fast carrier path owing to their ballistic transporting properties. Similar to the composite approach, nanometer dot doping (NDD) in the In₀.₇₄Zn₀.₂₆O/Zn₁₀₃₃O film allowed an increase in the conductivity of the channel layer and thus the carrier mobility of the resulting IGZO TFTs [73]. The coating of a self-organized polystyrene sphere and subsequent etching of the IGZO channel allowed a porous gate structure, which was used for the mask. The structure was treated with Ar plasma through a porous gate mask to increase the conductivity of the IGZO channel layer. This NDD on the IGZO channel region rendered a high mobility of 79.0 cm²Vs⁻¹ in the resulting TFTs, which can be attributed to the NDD-induced barrier lowering effect on the percolation conduction mechanism.

The stability near conduction band minimum of IGZO are believed to originate mainly from atomic dis-ordering. The excess oxygen or loosely bound oxygen species in the IGZO material can give rise to a substantial increase in the tailing state distribution. Zan et al reported an exceptionally high mobility of \(~100\) cm²Vs⁻¹ in amorphous In₀.₇₄Ga₁₀Zn₁₀₃₃O TFTs by capping the Ca/Al layer with subsequent stabilization in air [74]. The strong reduction power of the Ca film on the IGZO surface caused the elimination of interstitial oxygen defects in the IGZO channel, leading to a decrease in the tailing defect states. Interestingly, this high mobility in IGZO TFTs was achieved without compromising the SS factor or the \(\mu_{\text{on/off}}\) ratio. The device stored for 50 days in air exhibited a mobility of 105.7 cm²Vs⁻¹, SS factor of 0.12 V/decade and \(\mu_{\text{on/off}}\) ratio of \(~9\times10^6\), corresponding to the state-of-art characteristics in any TMO TFT (figure 11). Figure 12 shows the benchmark plot between the field-effect mobility and \(\mu_{\text{on/off}}\) ratio for various TMO TFTs. Because the values of the higher field-effect mobility would be compromised somewhat by the lower \(\mu_{\text{on/off}}\) ratios for various TMO TFTs, the regions of the TFTs satisfying the high mobility (>30 cm²Vs⁻¹) and \(\mu_{\text{on/off}}\) ratio (>10⁵) are still limited.

Note that some of the TMO TFTs referred in this section were not properly passivated. The adoption of a high quality passivation layer on the bare channel layer would further improve the PBS, NBS and NBIS stability of the resulting TMO TFTs [11, 75, 76].

### 3.2. BCE architecture for low fabrication cost

Bottom gate and ES type TMO TFTs exhibited good uniformity and stability as well as reasonable field-effect mobility because the electrical degradation of the channel properties, which is caused by physical and/or chemical damage during patterning of the source/drain (S/D) data line, can be prevented by the existing ES layer beneath the S/D metal film. This ES type device, however, has the drawback of relatively high processing cost and the difficulty in fabricating a short channel device. Compared to the BCE type structure, the ES type device requires additional deposition of an ES layer by PECVD as well as patterning by photo-mask lithography and etching. In addition, the existence of an ES layer on TMO semiconductor layer limits the definition of a short channel device due to the misalignment of the gate-to-ES or the source/drain-to-ES. The panel design with a bezel-free good form factor necessitates the addition of driver integration on the circuit peripheral region of the same panel, which requires the design of short channel (<2 μm) TFTs. For two main reasons, there is strong demand for BCE type TMO TFTs.

The S/D metal film on the channel layer should be over-etched during the patterning process of the S/D electrode line. The fabricated device showed simple conducting behavior because of the residual metallic components on the channel back surface. Dry etching or/and wet etching methods are used to pattern the S/D metal line. For a high-resolution AM display, dry etching would be preferred due to the ability of an anisotropic etching profile with good overlay accuracy. The first BCE IGZO TFTs-driven four inch AMOLED panel was fabricated by dry etching of the Mo S/D film on the IGZO contact layer using fluorine-based plasma [77]. On the other hand, the effects of plasma-based dry etching on the degradation of the resulting BCE IGZO TFTs was not addressed in detail. Park et al reported the effects of a N₂O plasma treatment and passivation layer on the device performance of the BCE IGZO TFTs [78]. The Mo S/D electrode
was patterned by dry etching using a SF$_6$/O$_2$ gas mixture. The transfer characteristics of the BCE IGZO TFTs were adversely affected by etching-induced damage. The SS factor and $I_{off}$ value were degraded to 1.0 V/decade and $10^{-11}$ A, respectively. This deterioration was attributed to the formation of oxygen loss and 3 nm thick in segregation, which might result from the selective removal of oxygen ions with the larger coordination number of the In cation. The device performance of the IGZO TFTs is also strongly dependent on the deposition conditions of the SiO$_2$ passivation layer. A huge hydrogen concentration, originating from the SiH$_4$ precursor, can be incorporated into the PECVD-derived SiO$_2$ film. Because hydrogen often acts as a shallow donor center in IGZO films, the thermal diffusion of hydrogen to the IGZO channel layer during post annealing results in metallic behavior of the resulting TFTs, as shown in figure 13(a). The switching property of the TFTs was improved substantially by the post treatment of N$_2$O plasma on the damaged channel surface, which supplied oxygen species near the IGZO back surface region and prevented the invasion of hydrogen from the SiO$_2$ passivation layer. Therefore, the N$_2$O treated device exhibited a high mobility of 37.0 cm$^2$/Vs, low SS of 0.25 V/decade and low $I_{off}$ of $10^{-13}$ A (figure 12(b)). The switching property and BTS induced stability of dry etching-based BCE IGZO TFTs can be improved further by optimizing the N$_2$O plasma treatment, deposition conditions and post annealing of the SiO$_2$ passivation layer [79].

The wet etching technique has the merits of low processing cost and relatively high throughput compared to dry etching. The selection and formulation of the wet etchant is of prime importance because ZnO-based oxide materials are etched too easily in weak acid. The effects of a HNO$_3$-based etchant and H$_2$O$_2$-based etchant on the performance of the IGZO TFTs with a Mo S/D electrode were compared [80].

<table>
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<th>Materials</th>
<th>Band gap (eV)</th>
<th>Electron affinity (eV)</th>
<th>References</th>
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<td>1.21 – 2.58 eV</td>
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</table>

Figure 10. (a) Schematic diagram showing the structure and band diagram of the ZnO/Al$_2$O$_3$ superlattice TFT. Transfer characteristics of TFTs with (b) single ZnO channel and (c) ZnO/Al$_2$O$_3$ superlattice channel. Reproduced with permission from [71].
The BCE IGZO TFTs using the HNO\textsubscript{3}-based etchant showed an inferior SS factor (1.22 V/decade) and more negative \(V_{\text{th}}\) value (1.8 V), indicating the formation of substantial etching-induced trap states near the IGZO back surface. From the O1s XP spectra, the oxygen-deficient region on the IGZO back surface was confirmed to have been created, which can be attributed to the surface reaction of IGZO films with a strong reducing agent containing H\textsuperscript{+} ions (pH < 1). In contrast, the \(H_2O_2\)-based etchant-patterned BCE IGZO device exhibited better switching characteristics: reasonable mobility of 13 cm\textsuperscript{2} V\textsuperscript{-1}s\textsuperscript{-1}, lower SS value of 0.74 V/decade and higher \(V_{\text{th}}\) of 2.6 V. The comparable performance using the \(H_2O_2\)-based etchant was previously reported for BCE IZO TFTs \[81\]. Therefore, the use of a \(H_2O_2\)-based etchant for patterning the S/D line in the BCE TMO TFTs would be a better choice than that of the HNO\textsubscript{3}-based etchant.

Recently, wet etching using a \(H_2O_2\)-based etchant and subsequent SF\textsubscript{6} plasma treatment to remove the wet-etching residues was attempted for BCE IZO TFTs with the Mo S/D electrode. The resulting BCE-type IZO TFTs exhibited stable behavior against external BTS applications: the \(V_{\text{th}}\) shift was only 0.25 and \(-0.2\) V under PBS and NBS conditions \((V_{\text{GS}} = \pm 30\) V, \(V_{\text{DS}} = 0\) V @60 C, 12 h), respectively \[82, 83\].

Although the TMO TFTs with Mo film as the S/D electrode have been studied intensively, there are a paucity of reports regarding the BCE processing for the Cu-contacted TMO TFTs. This needs to be investigated in the near future. Furthermore, the photo-bias instability of Cu contacted BCE TMO TFTs should be compared with its ES TMO TFT counterpart \[84\]. A future study should examine whether the reliability of BCE type TMO TFTs can be comparable to that of ES type TMO TFTs. Because TMO materials are vulnerable to various wet etchants and solvents as well as to ionic bombardment under a plasma ambient, the in-depth degradation chemistry of the underlying TMO materials during S/D patterning needs to be understood clearly. Obviously, the stoichiometry deviation and unwanted impurities near the back surface of the TMO films should be either eliminated or inactivated by developing novel post treatments or processing prior to the formation of a passivation layer, which would allow the ES type compatible reliability of the resulting ES type TMO TFTs.

### 3.3. Self-aligned coplanar architecture

Figure 14(a) shows the equivalent unit pixel circuit for AMLCD. When the scan signal switches from the turn-on state to the turn-off state, the pixel suffers from a certain voltage drop (\(\Delta V_{\text{P}}\)) due to capacitive coupling caused by the parasitic gate-to-source capacitance (\(C_{GS}\)) (figure 14(b)). The
The transient voltage drop can be given by the following equation:

$$\Delta V_P = \frac{C_{GS}}{C_{LC} + C_{SC} + C_{GS}} \Delta V_G,$$

where $C_{LC}$ is the capacitance of the liquid crystal, $C_{SC}$ is the capacitance of the storage capacitor and $\Delta V_G$ is the voltage swing of the scanning line. The imbalance in $V_P$ with frame inversion driving gives rise to flicker or image sticking, which is called the ‘kickback effect’ [85]. The kickback effect induces a similar image sticking problem in the panel driving of AMOLEDs. To reduce the kickback effect, the storage capacitance in one pixel should be increased. On the other hand, the higher resolution design renders a smaller unit pixel area, which limits the maximum storage capacitance.

Figure 13. (a) Transfer curve of a BCE type IGZO TFT after the S/D patterning and passivation patterning. (b) Transfer curve of a BCE type IGZO TFT after $N_2O$ plasma treatment. Reproduced with permission from [78].

Figure 14. (a) Equivalent unit pixel circuit of AMLCD (b) scan and pixel voltage variation during typical pixel driving in AMLCD.

The best way to eliminate the kickback effect is to adopt a self-aligned coplanar architecture. Although many studies of the staggered or inverted staggered structures of TMO TFTs have been reported, there are only a few reports of TMO TFTs with a self-aligned coplanar device. Morosawa et al reported the fabrication of IGZO TFTs with a self-aligned coplanar device for the first time [86]. Figure 2(c) shows a schematic cross-section of a self-aligned coplanar TFT. In terms of device operation, the modulation of the gate field-induced conductance in metal-insulator-semiconductor (MIS) capacitors is similar to that of the bottom gate configurations, such as BCE and ES structure. On the other hand, the charge carrier injection from the source to channel layer is limited due to a lack of overlap of the gate electrode and source electrode. Therefore, a key process in the self-aligned structure is to form a metal access layer, which is denoted by the pink color in figure 2(c). Although selective ion doping via the gate electrode and subsequent activation process are well established for coplanar LPTS TFTs, ion doping is unavailable for TMO TFTs. The authors introduced a metal reaction method to form a metallic IGZO access region (figure 15). The underlying mechanism is based on the thermodynamic equilibrium reaction between the capping metal layer and underlying IGZO layer. Two types of 5 nm thick capping layers, such as Ti and Al, were deposited by dc magnetron sputtering after patterning the gate line (see figure 15(b)). Subsequent thermal annealing in oxygen ambient at 300 °C caused the conversion from a metallic Al (Ti) film to an $Al_2O_3$ (TiO$_2$) film. During the metal reaction, the formation of $Al_2O_3$ near the Al/IGZO interface consumed the oxygen species from the back surface IGZO film, which gives rise to the creation of metallic IGZO due to an oxygen deficiency. The resulting self-aligned coplanar IGZO TFTs with a Mo/Al/IGZO contact stack exhibited a high mobility of 21.4 cm$^2$/Vs and a low contact resistance ($R_C$) of 2 $\Omega$cm, indicating good ohmic contact. The $R_C$ value of 2 $\Omega$cm was much smaller than those (20 $\sim$ 100 $\Omega$cm) reported for the bottom gate IGZO TFTs [87, 88].
Hydrogen doping of the TMO layer can be used to form a metallic access layer. SiO₂ or SiNₓ containing a large concentration of hydrogen species was deposited after patterning the gate bus line. During post deposition annealing, hydrogen diffuses in the S/D contact region of the IGZO layer, where the hydrogen incorporated in IGZO acts as a shallow donor. Therefore, the S/D contact region of IGZO converts to the metallic state, leading to ohmic contact between IGZO and the S/D electrode [89, 90]. The switching speed of the inverters based on the self-aligned coplanar a-IGZO TFTs was quite high (~1.25 MHz), which was attributed to the small parasitic capacitance and high mobility of 23.3 cm²Vs⁻¹ [90]. Finally, a plasma treatment, such as Ar, NH₃ etc, can be used for the formation of a metallic access region. As mentioned earlier, energetic ion bombardment, such as Ar radicals during plasma treatment, causes an oxygen-deficient region near the back channel surface of the TMO film, which results in a metallic region, presumably due to Vₒ₋₂-induced free electron generation [91].

Self-aligned coplanar TFTs with a channel layer of a-IZO electrode instead of a-IGZO was reported to have a high mobility of 157 cm²Vs⁻¹, low SS factor of 0.19 V/decade and good electrical reliability (figure 16) [92]. The N₂O plasma treatment facilitated a transition from the conducting IZO film to a semiconducting IZO due to the elimination of oxygen vacancies near the IZO back surface. Ohmic contact between the Mo S/D electrode and IZO channel layer was achieved by an Ar plasma treatment on the S/D contact region of the IZO film. Remarkably, the Vₒ₋₂ shift of the fabricated self-aligned device was ~0 and 1.0 V under severe NBIS and PBIS conditions (~3000 cd m⁻², VₒS,LST = ±20 V, VₒD,LST = 10 V @ 60 °C, 11 000 s), respectively.

The first self-aligned coplanar IGZO-driven AMOLED panel was demonstrated by Sony Inc., where a metallic access region was formed using an Al metal reaction method, (figure 17(a)) [86]. The 9.9 inch quarter high definition (960×540) AMOLED panel exhibited a brightness of 200 cd m⁻², a contrast ratio of 1 000 000:1 and a color gamut of 96%. In 2013, Bae and coworkers from LG display Inc. demonstrated a prototype of a 13.1 inch AMOLED panel that was driven by self-aligned coplanar IGZO TFTs (figure 17(b)). Metallic IGZO was formed by an Ar plasma treatment. The mobility, SS and Vₒ₋₂ values of the IGZO TFTs obtained in the OLED panel were 11.1 cm²Vs⁻¹, 0.12 V/decade and 0.92 V, respectively [93].

3.4. Cu process for low resistance S/D data line

The charging error in the storage capacitor of each pixel during the selection time increased with increasing resolution, frame rate and panel size, which gives rise to the shading effect and image distortion in the resulting display. To reduce this RC delay, the development of the gate and S/D interconnection process with a low resistivity as well as high mobility TFTs is essential. In this regard, the Cu metallization process in conjunction with the IGZO or non-IGZO semiconductor has been studied. In the case of the Cu gate line, the transitional process consisting of a Cu film, adhesion and/or diffusion barrier can be adopted in a straightforward manner because the Cu gate process is well proven in a-Si and LTPS technology. On the other hand, the application of a Cu film as the S/D data line satisfies the following requirements including good adhesion, excellent diffusion barrier properties and low ohmic contact between the TMO channel and Cu film.

The directly contacted device between the Cu electrode and IGZO channel suffers from the well-known Cu diffusion problem during elevated thermal annealing [94]. The hump-like behavior in the transfer characteristics of the Cu TFTs became dominant with increasing VₒS, which is believed to have originated from the electro-migration of Cu impurities along the channel length direction. The Cu impurity in the IGZO channel causes the creation of tailing trap states and deep states. From a comparative study of IGZO TFTs with an Al, Mo and Cu S/D electrode, the Cu contacted TFTs exhibited an inferior SS factor (~1.0 V/decade) to those (~0.5 V/decade) of Al or Mo contacted TFTs [95]. This can be explained by the inter-diffusion of Cu impurities into the IGZO channel region, which was confirmed by TOF-SIMS analysis. Therefore, the common feature of Cu-contaminated TFTs was the phenomena of severe stretch-out in the sub-threshold drain current due to the additional creation of Cu-related tailing states and deep states in the IGZO channel region [96]. Therefore, the diffusion barrier to prevent
Cu diffusion should be inserted between the Cu electrode and TMO channel layer.

Refractory metals, such as Ti, Mo, Cr, Ta or Mo-Ti alloy, can be used as a potential diffusion barrier and adhesion promoter for Cu-contacted TMO TFTs [97]. For example, the introduction of a Ta-diffusion barrier between the Cu electrode and ZTO channel layer can suppress the inter-diffusion of Cu impurities into the channel region during thermal annealing. The resulting Ta-inserted ZTO TFTs showed better switching properties than that of the Cu TFTs without a diffusion barrier: the mobility and $SS$ factor were improved from 13.2 cm$^2$ Vs$^{-1}$ and 1.1 V/decade (control device) to 18.7 cm$^2$ Vs$^{-1}$ and 0.48 V/decade, respectively [98]. Yun and Koike reported the fabrication of IGZO TFTs with a Cu–Mn alloy as the S/D electrode [99]. The good ohmic contact ($1.2 \times 10^{-4} \Omega\text{cm}^2$) between the Cu–Mn and IGZO film after annealing at 250 °C for 1 h was attributed to the formation of a metallic IGZO layer with a $N_c$ of $1.4 \times 10^{20}$ cm$^{-3}$, which allowed reasonable performance of the IGZO TFTs with the Cu–Mn S/D electrode: the mobility, $SS$ and $V_{th}$ were 10.8 cm$^2$ Vs$^{-1}$, 0.44 V/decade and 5.5 V, respectively. The Ti/Si stack barrier for the S/D Cu interconnection was examined. The good diffusion barrier properties and the contact resistance between IGZO and Cu metal resulted in reasonable performance of the resulting IGZO TFTs [100].

4. Conclusions

Vacuum-based n-type TMO TFTs have begun to penetrate as the backplane technology in commercial flat panel displays, such as AMLCD and AMOLED displays owing to their superior device properties and low fabrication cost, which is comparable to those of their silicon-based counterparts. To accelerate the implementation of TMO TFTs, a high mobility (>30 cm$^2$ Vs$^{-1}$) and low parasitic capacitance device architecture should be developed to compete with LPTS TFTs. Recently, various channel compositions, double channels or composite structures as approaches to achieving high mobility have been proposed. These approaches showed LPTS-compatible high mobility. On the other hand, the electrical reliability including the PBS, NBS, NBIS and hot carrier effect etc are not completely understood, which should be addressed in the near future. In terms of the device architecture, the current ES type bottom gate TMO TFTs is expected to be replaced by the BCE-type bottom gate and/or the self-aligned coplanar structure with a Cu interconnection because these structures have the merit of low cost fabrication, short channel device and low parasitic capacitance. Because the TMO composition and structure for high mobility (>30 cm$^2$ Vs$^{-1}$) should be compatible with advanced architectures, the issues related to the unit process and device integration for this purpose will become a major research topic.
aligned coplanar IGZO TFTs. Reproduced with permission from

References

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