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Effect of Channel Layer Thickness on Characteristics and Stability of Amorphous Hafnium–Indium–Zinc Oxide Thin Film Transistors

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We investigated the channel layer thickness dependence of the characteristics and stability in amorphous hafnium indium zinc-oxide (HIZO) thin film transistors (TFTs). HIZO TFTs were prepared with various channel thicknesses from 400 to 700 Å. In HIZO TFTs, carrier concentration is considerably high, which leads to channel layer thickness dependence. Threshold voltages of TFTs negatively shifted as the channel thickness increased. The threshold voltage shift at a high temperature is more severe in TFTs with thicker channel layers. The channel thickness dependence of the bias stability of HIZO TFTs is closely related to the back interface, rather than the bulk state.

1. Introduction

Recently, amorphous oxide-based thin film transistors (oxide TFTs) have gained considerable attention for their application in active-matrix displays. Oxide TFTs exhibit superior electrical properties, such as field-effect mobility or off-current level, compared with conventional amorphous silicon TFTs.1–3) The high electrical performance of oxide TFTs makes them one of the promising candidates for the backplane elements of ultrahigh-definition (UD) liquid crystal displays (LCDs) or active-matrix organic light emitting diode (AMOLED) displays.4–7)

Another important feature of oxide TFTs is their channel layer made of an amorphous phase.8,9) Although they show high mobility, they do not require the cumbersome recrystallization process, which causes a severe nonuniformity issue.10) Thus, oxide TFTs have potentially good uniformity, which is essential for large-area display production. However, in oxide TFTs, there is another issue that must be mitigated. Park et al.11) and Barquinha et al.12) reported that the channel thickness of oxide TFTs can be a very influential factor to electrical characteristics such as the threshold voltage (V_{TH}) of oxide TFTs, which means that the thickness variation may create non-uniformity in the electrical performance of oxide TFTs. Also, if there is a channel thickness dependence of electrical stability under the operating condition, nonuniformity issues, such as area-mura, might even be more severe.13) In this paper, we investigate the effect of channel thickness on the electrical characteristic and stability of amorphous hafnium–indium–zinc oxide (HIZO) TFTs under a high temperature (~250 °C) or electrical bias stress (V_G = 20 V).

2. Experimental Procedure

The amorphous HIZO TFTs with an etch stop layer were fabricated on glass substrates by a widely used hydrogenated amorphous silicon (a-Si:H) TFT-compatible process. Molybdenum was used as the gate material. The gate insulator was fabricated as SiO_2 employing plasma enhanced chemical vapor deposition (PECVD, 2000 Å). The amorphous HIZO layers with thicknesses of 400, 500, 600, and 700 Å were deposited by DC sputtering at room temperature. It was reported that adding the hafnium element can effectively control the carrier concentration and Hall mobility of the HIZO films.14) Hafnium may be a good substitute for gallium because of its higher affinity to oxygen than gallium.15) The ratio of HfO_2/In_2O_3/ZnO is 0.1 : 1 : 1. The X-ray diffraction (XRD) spectra of HIZO with various thicknesses were investigated and revealed it to be an amorphous phase, which implies that the nonuniformity issue due to phase is negligible. The SiO_2 etch-stop layer was fabricated by PECVD. Molybdenum was used as the source and drain material. A PECVD SiO_2 layer was employed for passivation (2000 Å).

3. Results and Discussion

3.1 Effect of channel thickness on characteristics of oxide TFTs

Figure 1(a) shows the I–V characteristics of fabricated HIZO TFTs with active layer thicknesses of 400 and 700 Å (V_DS = 10 V). Overall field effect mobility is about 9–10 cm^2/V·s. It should be noted that the off-current level was almost unchanged along with the active layer thickness, suggesting that the active layer is fully depleted.16) As shown in Fig. 1(a), as the active layer thickness increases, V_{TH} of the HIZO TFT decreases in the negative direction. Here, V_{TH} is defined as the gate voltage when the drain current is at 10^{-8} A. As the active layer thickness increases from 400 to 700 Å, the threshold voltage (V_{TH}) of the TFT decreases from 2.1 to −0.42 V. This phenomenon is reported in several works on IGZO TFTs or IZO TFTs and is quite interesting because a-Si:H TFT does not exhibit this tendency.11,12) V_{TH} of TFTs can be expressed as V_{TH} = q · D_H · (E_F - E_i)_{threshold}/C_i - Q_m/C_i + q · D_A · (E_F - E_i)_{threshold}/C_i + Δ_M, where C_i is the insulator capacitance, Q_m is the oxide charge density, D_H and D_A are the bulk trap density and the interface trap density, respectively, and Δ_M is the work function difference between metal/semiconductor. Note that, in the last term, it is described that the carrier concentration in the channel layers influences V_{TH}. D_H and D_A are the donor and acceptor concentrations, respectively (cm^{−2}). Since the HIZO layer is n-type, D_A is negligible and D_H is obtained by N_D · τ, where N_D is the donor concentration per unit volume. We calculated the carrier concentration N_D of 1.3 × 10^{17} cm^{−3}
Hall measurement was mental result because the carrier concentration obtained by $C/\text{14}$ and $230$ (TFTs with active layer thicknesses of 400 and 700 Å in Fig. 1(a), which shows a negative shift of can be well applied to our experimental results shown oxygen vacancies, which induce free carriers. This analysis associated with the generation of point defects, such as $V_{3.2}$ Effect of channel thickness on temperature stability of oxide TFTs on the basis of our experimental data, which shows a shift of 2.5 V for a channel thickness difference of 300 Å, which implies that the nonuniformity issue might be even more severe in oxide TFTs as the temperature increases.

3.2 Effect of channel thickness on temperature stability of oxide TFTs

Figure 1(b) shows the temperature-dependent $V_{TH}$ of oxide TFTs with thin (40 nm) and thick (70 nm) channel layers. It clearly shows that TFT with a thicker active layer shows stronger temperature dependence. A mechanism of the temperature-dependent characteristic of oxide TFT has been proposed in an early work by Takechi et al. The lower $V_{TH}$ observed with the increased temperature may be associated with the generation of point defects, such as oxygen vacancies, which induce free carriers. This analysis can be well applied to our experimental results shown in Fig. 1(a), which shows a negative shift of $V_{TH}$ with increasing temperature. In the case of increasing the channel thickness, the total amount of defects or charges in the bulk should also be increased; a thicker channel layer contains more point defects, such as oxygen vacancies, that potentially act as carrier generation sources. Thus, as the measured temperature increases, the $V_{TH}$ shift is more severe in the oxide TFTs with a thick channel layer. This result implies that the nonuniformity issue might be even more severe in oxide TFTs as the temperature increases.

3.3 Effect of channel thickness on bias stability of oxide TFTs

In order to investigate the device stability under bias stress, we have applied negative gate bias stress since the TFTs undergo negative gate bias during most of the operation time of an AMLCDD. We applied a gate bias of $V_{GS}$ of $-20$ V for 10,000 s in a dark state at room temperature. The source and drain contacts remained on the ground. We can observe that a $V_{TH}$ shift under bias stress shows a relationship with the active layer thickness, as seen in Fig. 2. Interestingly, the TFTs with thicker channels exhibit less degradation than those with thinner channels. This tendency is quite different from the result in Fig. 1(b), where TFTs with thicker channels seem to show more $V_{TH}$ shift under high temperature than those with thinner channels, owing to greater carrier generation. $V_{TH}$ degradation might conventionally be analyzed in terms of state creation or the charge injection theory, and it generally occurs in the front/back interface and/or channel bulk layer. While $V_{TH}$ is shifted under bias stress, other parameters such as S-slope and mobility do not show any degradation. This means that the $V_{TH}$ degradation is mainly caused by charge trapping rather than the creation of bulk trap states reported in other previous studies on oxide TFTs. Thus, bias stability analyses are more focused on charge trapping rather than carrier or state generation. We also checked out the XRD data of oxide layers with various thicknesses to confirm that the oxide layers are all amorphous and that there was no crystallization during growth. However, even though we exclude the creation of bulk state, the charge trapping mechanism near the dielectric/semiconductor interface is not sufficient to explain the $V_{TH}$ degradation with increasing channel thickness. Thus, the quality of the dielectric/semiconductor interface is not affected by channel thickness in the bottom gate structure.

Fig. 1. (Color online) (a) $I$–$V$ characteristics ($V_{GS}$ = 10 V) of HIZO TFTs with active layer thicknesses of 400 and 700 Å at room temperature and 230°C. (b) $V_{TH}$ of HIZO TFTs along with measurement temperature.

Fig. 2. (Color online) $V_{TH}$ shift of HIZO TFTs with various channel thicknesses under bias stress for 10,000 s.
where $E/C_2$ (Color online) Electric field under negative bias through oxide

**Fig. 3.** Jpn. J. Appl. Phys. (2008) 033502.

Therefore, as the last factor affecting the degradation, we consider the back interface between semiconductor/passivation layers. It is quite reasonable to consider that the effect of bias stress on the back interface is strongly related with channel thickness in the equation $E = V/d$, where $E$ is the gate electric field, and $d$ and $V$ are the channel thickness and bias, respectively. We carried out a device simulation using ATLAS (Silvaco) to investigate the electric field under the bias stress situation. Since the information on the sub-band gap of oxide TFTs is poorly estimated, we input several assumptions for the investigation of electric field.22,23) Our simulation model takes into consideration parameters, such as the affinity of 4.1 eV; the doping concentration of $4 \times 10^{16} \text{cm}^{-3}$; acceptor-like and donor-like tail states of $4 \times 10^{18} \text{cm}^{-3}$; and acceptor-like and donor-like Gaussian states of $5 \times 10^{16} \text{cm}^{-3}$. Figure 3 shows the electric field simulation profile under the bias stress ($-20 \text{V}$) situation along with the channel depth at the middle point between source and drain electrodes. Figures 3(a) and 3(b) clearly show that the electric field reaching the back interface decreases ($31 \to 7 \text{ kV/cm}$) as the channel thickness increases ($400 \to 700 \AA$), respectively.

Higher electric field results show that more electrons accumulated or were pushed near the back interface owing to bias stress. We consider the carrier trapping in the back interface between the semiconductor and the passivation layer or passivation layer, which leads to a change in the potential of the back interface. The lowered potential at the back interface causes $V_{TH}$ to shift negatively. Park et al. also found that $V_{TH}$ is shifted negatively as the electron concentration near the back interface increases, depleting the channel layer.20) Although both explanations contain several assumptions, they are considered to be reasonable explanations of the degradation of oxide TFTs in terms of $V_{TH}$.

4. Conclusion

We fabricated the HIZO TFTs with a bottom gate structure and investigated the stability of the TFTs. As the active layer thickness was increased, the $V_{TH}$ of the HIZO TFTs decreased mainly as a result of a high carrier concentration in the oxide channel layer. The temperature dependence was also influenced by channel thickness. Regarding the bias reliability ($-20 \text{V}$), the TFT with a thicker channel layer showed less $V_{TH}$ shift than the TFT with a thin channel layer.