High spatial density nanocrystal formation using thin layer of amorphous Si 0.7 Ge 0.3 deposited on SiO₂

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High spatial density nanocrystal formation using thin layer of amorphous Si$_{0.7}$Ge$_{0.3}$ deposited on SiO$_2$

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The process to make nanocrystals with an average size <5 nm and a spatial density >10$^{12}$/cm$^2$ was proposed using agglomeration and partial oxidation of thin amorphous Si$_{0.7}$Ge$_{0.3}$ layer deposited in between the SiO$_2$ layers by low pressure chemical vapor deposition. The reason to use an amorphous layer is to make it possible to deposit a thin continuous layer with a thickness of less than 5 nm. Si$_{0.7}$Ge$_{0.3}$ alloy layer was used to control the threshold density of the nanocrystals by using selective oxidation of Si in Si$_{0.7}$Ge$_{0.3}$ alloy layer. The single electron memory, similar to a flash type memory device was fabricated using these Si$_{0.7}$Ge$_{0.3}$ nanocrystals. The Coulomb blockade effect could be clearly observed at room temperature with a threshold voltage shift of about 2.4 V, which demonstrated the formation of nanocrystals with a high spatial density. © 2000 American Institute of Physics. [S0021-8979(00)06405-7]

I. INTRODUCTION

A single electron device operated by the Coulomb blockade effect is actively investigated as one of the strongest candidates for future nanoscale electronic devices.1,2 Until now, various device structures have been proposed employing the idea of the coulomb blockade effect.3–5 Among these device structures, Tiwari et al.5 proposed the single electron device using nanocrystals incorporated in the gate oxide as a floating gate like flash type memory device. This can be used for a single electron memory device by the discrete threshold voltage shift resulting from the charging of an electron in each nanocrystal. The threshold voltage shift in this type of device is expressed as

$$\Delta V_T = \frac{q n_{dot}}{\epsilon_{ox}} \left( \frac{1}{t_{ctl} \epsilon_{ox} \epsilon_{Si}} + \frac{1}{2 d_{dot} \epsilon_{Si}} \right).$$

(1)

where $\Delta V_T$ is the threshold voltage shift, $t_{ctl}$ is the thickness of the oxide in between the nanocrystals and control gate, $d_{dot}$ is the diameter of nanocrystal, $\epsilon_{ox}$ and $\epsilon_{Si}$ are the permittivity of oxide and Si, respectively, and $n_{dot}$ is the density of nanocrystals. As shown in Eq. (1), the shift in threshold voltage is proportional to the density of nanocrystals. Thus, a high density of nanocrystals is needed for a large shift in threshold voltage. In particular, the size of the nanocrystals must be less than a few nanometers for room temperature operation since the total capacitance must be <3.9 aF at room temperature in order to prevent charging of the electron by thermal fluctuation.

In this respect, the formation of nanocrystals on an amorphous dielectric material is a critical process for the fabrication of a single electron device. Until now, various methods have been proposed to make nanocrystals in the gate oxide.6,9,10 For instance, Nakajima et al.6 made Sn nanocrystals in SiO$_2$ with an average size of about 5 nm. They employed Sn ion implantation at a low energy of 10 keV with a dose of 5×10$^{13}$ ions/cm$^2$ in a 15 nm thick SiO$_2$ gate oxide with subsequent thermal annealing at 900 °C for 10 min in a N$_2$ environment. Also, Classen and Bloem7 and Kato et al.5 employed the initial stage of the polycrystalline Si deposition during low-pressure chemical vapor deposition (LPCVD) to fabricate nanocrystals with a size <10 nm and spatial density of approximately 10$^{11}$/cm$^2$. Kim et al.9 also employed the similar process, but they introduced HF dipping of the oxide layer before deposition of crystalline Si nanocrystals to increase the nucleation sites. With this process, they made as-deposited Si nanocrystals with a height of about 4 nm and diameter of about 10 nm with a spatial density of 5×10$^{11}$/cm$^2$. King et al.10 made Ge nanocrystals through the sequential thermal oxidation of the Si$_{1-x}$Ge$_x$ layer at various temperatures by the selective oxidation effect of Si$_{1-x}$Ge$_x$ layer oxidation. They formed Ge nanocrystals with the size of about 3 nm and spatial density of about 3.5×10$^{12}$/cm$^2$ by sequential oxidation of the Si$_{1-x}$Ge$_x$ layer which was formed by Ge implantation in Si and high temperature annealing. With this process, they demonstrated a
flash type single electron memory device with a 0.4 V threshold voltage shift at room temperature.

In this study, the agglomeration and partial oxidation of as-deposited amorphous Si$_{0.7}$Ge$_{0.3}$ thin layer were used to make nanocrystals with a small size and high spatial density. Especially, it is thought that the wide process window for the control of nanocrystal density can be easily obtained by using the selective oxidation of Si in the Si$_{1-x}$Ge$_x$ oxidation process. Also, the single electron memory device similar to the flash type memory device was fabricated with these processes and the Coulomb blockade effect was observed at room temperature.

II. EXPERIMENT

Amorphous Si$_{0.7}$Ge$_{0.3}$ (~4 nm) thin layer was deposited on 4-nm-thick thermally grown SiO$_2$. The Si$_{0.7}$Ge$_{0.3}$ layer was deposited using Si$_2$H$_6$ and GeH$_4$ at 375 °C, 1 Torr. Detailed information about the low-pressure chemical vapor deposition of Si$_{1-x}$Ge$_x$ was previously reported. After deposition of the amorphous Si$_{0.7}$Ge$_{0.3}$ (~4 nm) layer, SiO$_2$ was deposited to a thickness of 18 nm by LPCVD using Si$_2$H$_6$ and O$_2$ gases at 375 °C, 1 Torr. This structure of CVD SiO$_2$ (18 nm)/amorphous Si$_{0.7}$Ge$_{0.3}$ (~4 nm)/thermal SiO$_2$ (4 nm) on Si was annealed at 800 °C for 10 min either in a purged N$_2$ environment in a conventional atmospheric quartz tube furnace, or in a vacuum. The vacuum level was <10$^{-8}$Torr. These nanocrystals were characterized using conventional and high-resolution transmission electron microscope (TEM).

After the formation of the gate oxide consisting of thermally grown tunneling SiO$_2$ (~4 nm), Si$_{0.7}$Ge$_{0.3}$ nanocrystals, and upper control SiO$_2$ (~18 nm) deposited by LPCVD, this structure was annealed at 700 °C for 30 min in an O$_2$ environment to improve the dielectric quality of the upper control SiO$_2$ deposited by LPCVD. With this structure, the flash memory type single electron device was fabricated based on the standard NMOS process. The channel length and width of this device is 1 and 10 μm, respectively. After phosphorous-doped poly-Si gate patterning, arsenic was implanted to form n$^+$ source/drain region. After ion implantation, annealing was carried out at 900 °C for 20 min in a N$_2$ environment. The devices were characterized using HP4155A semiconductor parameter analyzer. During write operation, the drain was biased at 0.1 V and a single programming pulse was applied. After each write/erase operation, the threshold voltages of written/erased devices were extracted from the subthreshold characteristics at a constant current of 10 nA. All the electrical characteristics were measured at room temperature.

III. RESULTS AND DISCUSSION

Figure 1 shows the cross-sectional TEM bright-field image of the as-deposited CVD SiO$_2$ (18 nm)/amorphous Si$_{0.7}$Ge$_{0.3}$ (4 nm)/thermal SiO$_2$ (4 nm) structure on Si substrate. The TEM micrograph does not show the amorphous Si$_{0.7}$Ge$_{0.3}$ layer as a flat surface. This structure was further analyzed by using high-resolution TEM to ascertain whether the amorphous Si$_{0.7}$Ge$_{0.3}$ layer was deposited as fully continuous layer or islands. Figure 2 shows the cross-sectional high-resolution TEM image of the above structure. This figure indicates that the as-deposited Si$_{0.7}$Ge$_{0.3}$ was deposited as isolated islands with the size of about 4 nm. For the confirmation of the exact size and the spatial density of the Si$_{0.7}$Ge$_{0.3}$ islands, plan-view TEM analysis was carried out after annealing at different annealing conditions, whose results are shown in Fig. 3.

Figure 3(a) is the plan-view TEM bright-field image of nanocrystals annealed at 800 °C for 10 min in a vacuum environment. This figure shows that the Si$_{0.7}$Ge$_{0.3}$ was separated individually with the average diameter of isolated nanocrystals about 3.6 nm and the spatial density is approximately 1.5×10$^{12}$/cm$^2$. Figure 3(b) is the plan-view TEM bright-field image of nanocrystals annealed at 800 °C for 10 min in a purged N$_2$ environment. This figure shows that the average diameter of Si$_{0.7}$Ge$_{0.3}$ nanocrystals is about 5 nm and their spatial density is about 3.8×10$^{11}$/cm$^2$ which is lower than that of nanocrystals annealed in a vacuum by approximately four times. The result of high-resolution TEM ana-
sis of Si$_{0.7}$Ge$_{0.3}$ nanocrystals annealed in a purged N$_2$ environment, shown in Fig. 4, shows that the diameter of nanocrystals is $\leq 5$ nm.

The fact that the density of nanocrystals annealed in a purged N$_2$ environment is lower than that of nanocrystals annealed under vacuum is thought to be due to the partial oxidation of Si$_{0.7}$Ge$_{0.3}$ either by oxygen or moisture in the furnace during annealing in a purged N$_2$ environment. According to the results of the oxidation of Si$_{1-x}$Ge$_x$ alloy reported by Holland et al.\textsuperscript{12} and Nayak et al.\textsuperscript{13} Si is preferentially oxidized and Ge is piled up during oxidation. Therefore, it seems to be possible that one can control the density of Si$_{0.7}$Ge$_{0.3}$ nanocrystals by varying the oxidation condition to a certain degree. Also, by introducing the CVD SiO$_2$ capping layer on the Si$_{0.7}$Ge$_{0.3}$ layer, it is possible to obtain a wider process window for partial oxidation than without a CVD SiO$_2$ capping layer.

Figures 5(a) and 5(b) exhibit the analytical data showing the average size and spatial density of Si$_{0.7}$Ge$_{0.3}$ nanocrystals annealed under vacuum. The spatial density was measured by counting the number of sections divided by 100 nm $\times$ 100 nm area within which the number of nanocrystals was different. The average diameter of nanocrystals is approximately 3.6 nm and the standard deviation is about 1.3 nm. The spatial density of nanocrystals is about $1.5 \times 10^{12}$/cm$^2$ and the standard deviation is $9 \times 10^{10}$/cm$^2$, which is about 6%. Figures 6(a) and 6(b) are those of Si$_{0.7}$Ge$_{0.3}$ nanocrystals annealed in a purged N$_2$ environment. The average diameter of nanocrystals is about 4.9 nm and the standard deviation is about 1.3 nm. The spatial density of nanocrystals is about $3.8 \times 10^{11}$/cm$^2$ and the standard deviation is $3.5 \times 10^{10}$/cm$^2$, which is approximately 9.3%.

FIG. 3. Plan-view TEM bright-field images of Si$_{0.7}$Ge$_{0.3}$ nanocrystals; (a) annealed at 800 °C for 10 min at vacuum environment, (b) annealed at 800 °C for 10 min at the purged N$_2$ environment.

FIG. 4. Plan-view high-resolution TEM image of Si$_{0.7}$Ge$_{0.3}$ nanocrystals annealed at 800 °C for 10 min at the purged N$_2$ environment.

FIG. 5. (a) Size distribution and (b) spatial distribution of nanocrystals annealed at 800 °C for 10 min at vacuum environment.
In both cases, the average diameter of Si0.7 Ge0.3 nanocrystals is below 5 nm and the standard deviation of nanocrystal size is below 2 nm. In addition, the spatial density varies from about 1011 /cm^2 to 1012 /cm^2 as a function of the annealing condition, with a standard deviation of less than 10%. The fact that the deviation of the spatial density of nanocrystals is below 10% means the deviation of the threshold voltage shift is also below 10% if the other parameters are the same. This is because the threshold voltage shift is linearly proportional to the density of nanocrystals, as shown in Eq. (1).

From the results shown above, it can be found that the as-deposited amorphous Si0.7 Ge0.3 layer was not deposited as a continuous layer contrary to our expectations. This is thought to be due to the thickness of the Si0.7 Ge0.3 layer being too thin to make the substrate surface fully covered by adatoms deposited by LPCVD. At the initial stage of deposition of the crystalline phase, it is well known that isolated islands are formed because the adatoms deposited on the substrate can migrate to form stable nuclei. Also, following adatoms can migrate to the existing nuclei and increase the size of cluster to minimize the total energy. This is probable in the crystalline phase deposition because the surface diffusion of adatom occurs due to the high temperature of substrate. But, in the chemical vapor deposition of amorphous thin films, it is thought that the surface diffusion length of adatoms is too small to form the stable nuclei after they arrive on the substrate. Nevertheless, isolated islands can be formed in amorphous layer deposition, as shown in our results. This isolated islands formation is thought to be due to the preferential decomposition of the Si and Ge precursor on predeposited atoms. This preferential decomposition can occur by direct attachment and decomposition of the precursor on predeposited atoms from the vapor phase or by surface diffusion of the precursor, not adatom, on the substrate. In Si or Si1-x Ge_x CVD, the preferential deposition of Si or Si1-x Ge_x on Si rather than on SiO_2 was reported and this tendency was clearly observed at the higher Ge concentration. This means that the precursor of Si or Ge can be preferentially decomposed on predeposited Si or Si1-x Ge_x atoms rather than on the SiO_2 substrate. Therefore, the island formation of amorphous Si1-x Ge_x is thought to be due to the preferential decomposition of Si and Ge precursors on predeposited atoms. Also, experimental results show that the spatial density of nanocrystals which is deposited as an amorphous state is larger than that of crystalline nanocrystals reported by other researchers. This is thought to be due to the smaller critical size of an amorphous stable cluster than that of a crystalline cluster and insufficient surface diffusion length of adatoms for the growth of the cluster. Thus, the higher spatial density of islands with the smaller size in amorphous phase deposition can be obtained rather than a smaller spatial density of islands with the larger size in the crystalline phase deposition.

By using this method, a flash type single electron memory device was fabricated. The Coulomb blockade effect of single electron memory characteristics is clearly observed in Fig. 7. After programming, two levels of threshold voltage plateau as a result of the charging of one and two electrons, respectively, are shown. Programming voltage was varied from 0 to 12 V and programming time was 50 s. The long programming time was needed for electron charging in nanocrystals located in gate oxide because the thickness of the tunneling oxide is 4 nm, which is too thick for instant tunneling by applied programming voltage. The first and second threshold voltage shift is 3.4 and 2.4 V, respectively. The reason why the threshold voltage shift is different after between first charging and second charging is not fully un-
derstood, but this difference is thought to be originated from the hole injection during the erase operation. From this consideration, the more acceptable value of the threshold voltage shift is 2.4 V because this value shows the pure difference after between charging of one and two electrons in nanocrystals. From this consideration, the more acceptable value of the threshold voltage shift is 2.4 V because this value shows the pure difference after between charging of one and two electrons in nanocrystals. From the threshold voltage shift after charging of the electron in the nanocrystals and dimension of this device, the size and spatial density of nanocrystals can be calculated by Eq. (1). If the diameter of nanocrystals is 5 nm, the spatial density of nanocrystals can be deduced to be about $3 \times 10^{12}/\text{cm}^2$, which is consistent with TEM analysis and a value large enough for practical applications.

IV. CONCLUSION

By using amorphous Si$_{0.7}$Ge$_{0.3}$ deposited by LPCVD, it is possible to make nanocrystals whose average diameter is $<5$ nm with a spatial density $>10^{12}/\text{cm}^2$. Additionally, the density of nanocrystals can be easily controlled by varying the annealing conditions with Si$_{0.7}$Ge$_{0.3}$ nanocrystals due to the selective oxidation of Si during the Si$_{0.7}$Ge$_{0.3}$ oxidation process. Therefore, nanocrystal formation using the as-deposited amorphous Si$_{0.7}$Ge$_{0.3}$ is thought to be a more promising technique for the formation of nanocrystals, having small size and high spatial density than using as-deposited crystalline Si nuclei. With this process, it is possible to make the flash type single electron memory device.

Two levels of threshold voltage shift are clearly observed and the magnitude of the threshold voltage shift is about 2.4 V resulting from the high spatial density of nanocrystals, which is high enough for the practical operation of the device.