

SiO$_2$ Film Formed by Inductivity Coupled Plasma Chemical Vapor Deposition at Low Temperature for Poly-Si TFT

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In this study, silicon dioxide (SiO$_2$) films were deposited at temperatures below 200$^\circ$C by using the inductivity coupled plasma chemical vapor deposition (ICP CVD) technique. The breakdown electric field of as-deposited SiO$_2$ film by using this method shows values as high as 8.6 MV/cm. Additionally the effects of post-metallization annealing on SiO$_2$ were investigated. After 400$^\circ$C annealing, the capacitance-voltage (C-V) characteristics such as flat-band voltage, and interface trap density are improved considerably. In TFTs fabricated on single crystal SOI substrates at low temperatures below 400$^\circ$C by using this gate dielectric, a sharp gate voltage swing of 85 mV/dec. with high electron mobility was obtained. ICP CVD, by using high density plasma, can realize an excellent SiO$_2$ film and is expected to be applicable for the gate oxide in high performance Si TFT on plastic as well as on glass substrate.

PACS numbers: 42.30.R, 42.40.Ht, 42.30.Kq

Keywords: Gate insulator, SiO$_2$, ICP CVD, High density plasma

I. INTRODUCTION

Recently, flat panel displays on plastic substrate have attracted considerable attention due to robustness, light-weight and flexibility. Low-temperature formation of high-quality gate oxide is one of the key issues to realize micro-electronics on plastic as well as on glass substrate. The main properties that make SiO$_2$ a reliable gate dielectric are low leakage current, high breakdown voltage, and low interface trap density. In addition, a low deposition temperature below 200$^\circ$C is required for the poly-Si TFT on a flexible panel [1]. These characteristics are dependent on the Si/O ratio, hydrogen content, and deposition method. Conventional SiO$_2$ formation techniques include thermal oxidation, LP (Low-Pressure) CVD (Chemical Vapor Deposition) and PE (Plasma-Enhanced) CVD etc. Thermal gate oxide has good electrical characteristics, but it requires a high temperature ($\sim$ 1000 $^\circ$C), which is not compatible with flexible poly-Si TFTs. The PECVD technique is able to reduce the deposition temperature ($< 400$ $^\circ$C). However, the resultant properties are not at acceptable level for TFT applications using lower temperature processes, as the PECVD silicon dioxide is not confined to the stoichiometric SiO$_2$ composition, as it contains amounts of bonded hydrogen [2,3].

There is considerable interest in dielectric films that can be deposited at temperature lower than 400$^\circ$C. Recently, the ECR (Electron Cyclotron Resonance) microwave CVD technique has been developed and has deposited SiO$_2$ films with good quality [4,5]. The ICP CVD technique has also been developed [6]. The advantage of ECR CVD or ICP CVD systems over the conventional PECVD system is the ability to realize high-density plasma, as well as low deposition pressure and temperature. These process parameters will result in minimizing film contamination, promoting film stoichiometry, and reducing radiation damage caused by direct ion-surface interaction. The ICP CVD system has further advantages, such as ability to produce uniform plasma over large-diameter substrate and to make a compact and simple source while reducing the plasma damage to the film [7]. For the ICP CVD film by using HDP (High Density Plasma), some potential advantages are known such as lower hydrogen content, void-free gap filling of high aspect ratio features, self-planarization, and high deposition rate at low temperature ($< 200$ $^\circ$C).

Even though there have been a few reports on the properties of SiO$_2$ film deposited by using ICP CVD, they do not focus on the electrical properties such as breakdown field and flatband voltage which are indispensable properties for gate insulator of electronic devices [8]. In this work, we have studied the electrical and optical properties of SiO$_2$ gate dielectric layers deposited...
by ICP CVD in both MOS (metal-oxide-semiconductor) and SOI TFT (silicon on insulator thin film transistor) devices.

II. EXPERIMENTS

A schematic diagram of the ICP CVD system is shown in Figure 1. In order to deposit films over a large area uniformly, the system was designed with a planar type of plasma source with a specific shower head. The substrates used in this study were B-doped p-type Si wafers. The substrate temperature was measured by using a thermocouple attached on the wafer, giving results as shown in Figure 2. Even if the substrate heater is not activated, the substrate temperature increases as high as 170 °C by plasma irradiation. In this self-heated condition, which corresponds to a regime of lower pressure and higher power, the deposition is controlled at the rather lower growth rate of 0.4 Å/s below 200 °C, the film is expected to become dense and to receive less damage by rf plasma. For this work, the ICP source power and the working pressure were fixed at 1000 W and 15 mTorr, respectively. Reactant gases of SiH₄ and O₂ diluted by Ar were used for the SiO₂ formation. The gas flow ratio of O₂/SiH₄ was kept at about 13. The 100 nm thick silicon dioxide (SiO₂) films were deposited at temperatures below 200 °C. Deposition rate and uniformity were determined by ellipsometer measurements.

For measurement of I-V and C-V characteristics, a MOS capacitor was fabricated with the deposited oxide film on a Si wafer. Aluminum dot electrodes, 0.04 cm in diameter, were deposited by e-beam evaporation. After that, a post sintering annealing was carried out in nitrogen ambient with an annealing temperature below 400 °C. The C-V characteristics were measured at high frequency (1 MHz) by using a LCR meter (HP 4284). The I-V characteristics were obtained (by using a Keithley 288 probe station) to investigate the leakage current behavior. In order to know the SiO₂ network and its bonding structure, infrared measurements were performed with a FTIR (Fourier Transform Infra-Red) spectrometer (Nicolet 205) by using a nominal resolution of 4 cm⁻¹ of 120 scans to average the data.

Finally, in order to confirm the properties of the film as a gate oxide, TFT devices were fabricated at low temperature below 400 °C by using thin SOI (Silicon on Insulator) substrate, and the interface properties related to the device performance were evaluated.

III. RESULTS AND DISCUSSION

The composition, hydrogen content and bond configuration of the films were estimated roughly by infrared transmission spectra. Figure 3 shows the typical infrared (IR) spectrum for SiO₂ deposited by ICP CVD at 150 °C. The spectrum shows absorption peaks around 1054 and 808 cm⁻¹, associated, respectively, with stretching and bending fundamental vibration modes of Si-O bonds. There are no absorption features located at frequencies between 3350 and 3600 cm⁻¹, or at 925 cm⁻¹, that are characteristic of the vibration modes of Si-OH groups [9]. The absence of any absorption peak associated with Si-H...
Fig. 4. (a) J-E characteristic of silicon dioxide film deposited by ICP-CVD, and (b) Variation of VFB with post annealing temperature.

Fig. 5. SOI TFT transfer curve (\(t_{ox}=21\) nm, \(t_{si}=50\) nm, \(W/L=20/8\)).

groups in the SiO\(_2\) films, whose stretching and bending bands are located at 2260 and 880 cm\(^{-1}\), respectively, has been confirmed as well [10]. As the hydrogen content is below the IR detection limit, we can speculate that the obtained SiO\(_2\) film contains less hydrogen and is more dense in the network than the film formed by conventional PE CVD.

Figure 4(a) shows a typical J-V curve for SiO\(_2\) obtained by ICP CVD, compared to that of thermal oxide. The breakdown field obtained is about 8.6 MV/cm, which was defined as the field at which the leakage current density is 1 \(\mu\)A/cm\(^2\), and the current density measured at 1 MV/cm is about \(1 \times 10^{-8}\) A/cm\(^2\). The leakage current density of ICP CVD SiO\(_2\) is even higher than that of the thermally grown oxide.

The flat-band voltage obtained by C-V measurement shows -1.5 V due to damage during deposition of metal electrode by e-beam. The damage can be eliminated by a post annealing at 400 °C after metallization, as shown in Figure 4(b). The SiO\(_2\) films were annealed at various temperatures in a nitrogen environment for 20 min. As the annealing temperature increases, the C - V characteristics such as flat-band voltage improve considerably. The flat-band voltage at annealing temperature of 200 °C and 400 °C were measured by -2 V and -0.2 V respectively. It is considered that these electrical properties of ICP CVD SiO\(_2\) are sufficiently acceptable for use as gate insulators of electronic devices such as TFT.

Finally, in order to evaluate the possibility of application as a gate oxide in devices, TFTs were fabricated by using 200 nm thick ICP SiO\(_2\) on single-crystal SOI substrate by using a low temperature process below 400 °C, and the electrical characteristics were evaluated as shown in Figure 5. A high performance transfer curve with a sharp gate voltage swing of 85 mV/dec., and a high mobility of 707 cm\(^2\)/Vs. was obtained, even in the case of the low temperature gate oxide. This result shows that the film is dense and has a low population of interface-trap densities, which is the advantage of ICP CVD, and the SiO\(_2\) film should be applicable to low temperature TFT devices

IV. CONCLUSION

In this study, SiO\(_2\) films were deposited below 200 °C by using ICP CVD. The breakdown electric field attained was as high as 8.6 MV/cm, and the C-V characteristic indicates that interface trap density is reduced considerably. By fabricating a TFT by using SOI substrate at low temperature below 400 °C, a sharp gate voltage swing of 85 mV/dec. with high mobility was obtained. ICP CVD with low temperature deposition by using a high density plasma can realize an excellent SiO\(_2\) film, and is expected to be applicable to high performance Si TFTs on plastic as well as on glass substrates.

REFERENCES