Ultra-Low Temperature Poly-Si Thin Film Transistor for Plastic Substrate

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We studied the fabrication of poly-Si TFT (thin film transistor) by using excimer laser crystallization of sputtered a-Si film at below 200 °C. We could obtain the precursor a-Si film with low impurity gas content of 0.39 % by using Xe sputtering and poly-Si film with maximum grain size of 1 µm. We successfully fabricated poly-Si TFT with a field-effect mobility of 70 cm²/V·sec on glass and 15 cm²/V·sec on plastic by using ultra low temperature process at below 200 °C, respectively.

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I. INTRODUCTION

Flexible displays on plastic substrates, using polycrystalline Si (poly-Si)-based thin film transistor (TFT) devices to drive either active matrix liquid crystal displays (AMLCDs) or active matrix organic light emitting diode (AMOLED) displays are expected to be a driving force of the display industry in the near future. The main challenges that are anticipated in the manufacture of poly-Si TFTs on plastic are the deposition of the precursor a-Si and the crystallization of this layer at temperatures compatible with the plastic substrates generally below 200 °C [1–4]. Excimer laser crystallization (ELC), using high-power pulses of a short duration of several tens of nanoseconds, has emerged as an alternative method for crystallizing a-Si films, as it can efficiently melt the Si film at the surface while minimally affecting the substrate [5]. While chemical vapor deposition (CVD) methods have been used successfully to deposit a-Si films on glass substrates, they inherently incorporate hydrogen gas during the deposition process, which may explosively release during ELC. Sputtering is considered an ideal method of depositing a-Si precursor material because it may be conducted at room temperature and does not incorporate hydrogen [6–8]. However, the sputtered a-Si film also has the problem of film delamination during ELC at higher laser energy densities. Some reports explain that this delamination is due to film ablation by explosive evolution of captured Ar gas [9]. In this work, we studied a new and effective method for reducing incorporated impurity gas content, and obtained extremely large grain poly-Si film and fabricated poly-Si TFT with mobility sufficient to drive AMOLED on both quartz and plastic substrates in a process at below 200 °C.

II. EXPERIMENTS

The substrates used in this study are quartz and plastic substrates, 200-µm PES with organic coating layer on both sides, for LTPS use. In the case of plastic substrate, before deposition of the a-Si layer, two types of intermediate buffer layers were deposited between the plastic substrate and the Si film: firstly, 100-nm thick AlN and secondly, 200-nm-thick SiO2. The SiO2 layers were deposited by a low-temperature (170 °C) inductively-coupled plasma CVD (ICP-CVD) method, while the AlN layer was deposited by reactive sputtering of Al in an N2 atmosphere. The inclusion of a high-thermal-conductivity layer such as AlN in the buffer layer stack is thought to increase the laser energy density that is tolerated by the a-Si film by alleviating thermal interlayer stress, among the various mechanisms that possibly contribute to the film delamination during ELC [10].

A 50-nm-thick a-Si layer was deposited by using rf sputtering at 200 W with Ar or Xe plasma [11]. The pressure of the sputtering gas was kept at 0.67 Pa, and the deposition rate was approximately 0.1 nm/sec when using Ar gas, or 0.05 nm/sec when using Xe gas. The a-Si film was crystallized by ELA by using a XeCl (308 nm) laser and the resulting microstructures were analyzed by scanning electron microscopy (SEM).

The crystallized Si film was patterned into the island structure depicted in Figure 1(c) by using mask lithogra-
Fig. 1. Process flow of poly-Si TFT fabrication on quartz and plastic substrates.

The SiO$_2$ for the gate insulator material and Al:Nd for the gate electrode material were deposited by using ICP-CVD [12] and sputtering, respectively. The same films were deposited on Si wafer substrates to form Metal Oxide Semiconductor (MOS) capacitors, for analysis of the leakage and C-V characteristics.

A second mask was used to pattern the SiO$_2$ and Al:Nd films into the gate stack. Afterwards, the source and drain were doped by using ion implantation at a dose of $5 \times 10^{15}$ cm$^{-2}$ and activated by using excimer laser irradiation with low energy density of 150 mJ/cm$^2$.

The device characteristic of the n-type TFTs was analyzed by measuring the basic transfer curve, and the field effect mobility of the channel was calculated.

III. RESULTS AND DISCUSSION

Figure 2 shows RBS data revealing both the Ar content and the Xe content in the sputtered a-Si films attained by each case of Ar sputtering and Xe sputtering. The incorporated Ar content in the a-Si films by Ar sputtering is 1.1 % and the incorporated Xe content in the a-Si films by Xe sputtering is only 0.39 at.%. Generally, it is not avoidable that inert gas used for plasma ignition and target sputtering is incorporated. It is thought that the most acceptable process among possible capturing scenarios of inert gas is an elastic collision of neutral atoms of inert gas and Si particles accelerated from target to substrate. The mass of Xe gas is about 3 times that of Ar gas. Therefore, in the case of Xe sputtering, it is more difficult to obtain sufficient energy to incorporate Xe gas within the a-Si film by collision of accelerated Si particles. The a-Si film by heavy Xe gas sputtering can be expected to attain less captured gas than that by light Ar gas sputtering. Figure 3 shows a SEM image of the poly-Si film. This poly-Si film is obtained by ELA of Xe sputtered a-Si film with post-annealing during 2 hr at 200 °C. The average grain size is 0.5 µm and the maximum is larger than 1.0 µm, as shown in the SEM image [11]. The current-leakage behavior of the ICP-CVD dielectric is shown in Figure 4. The gate oxide film, which is deposited on c-Si wafer by using ICP-CVD with a high-density plasma below 200 °C, exhibits a high breakdown voltage of over 8 MV/cm, due to its smooth Si/SiO$_2$ interface with a low interface trap density and fewer hydrogen-induced carrier trapping sites [12]. Typical transfer characteristics of the fabricated n-channel TFTs are shown in Figure 5.
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Fig. 4. J-E characteristics of SiO$_2$ film by using ICP-CVD at 170 °C.

![Graph](image)

Fig. 4. J-E characteristics of SiO$_2$ film by using ICP-CVD at 170 °C.

Fig. 5. Log $I_D$-$V_g$ transfer characteristic and field effect mobility of poly-Si TFT (a) on quartz and (b) on plastic substrate [6] at below 200 °C.

![Graph](image)

Fig. 5. Log $I_D$-$V_g$ transfer characteristic and field effect mobility of poly-Si TFT (a) on quartz and (b) on plastic substrate [6] at below 200 °C.

measured field-effect carrier mobility of the poly-Si TFT on quartz and plastic substrate is 70 cm$^2$/V·s and 15 cm$^2$/V·s, respectively [13]. Although other electrical parameters such as $I_{on}/I_{off}$ ratio are also important for display application, with regard to mobility, the performance of this poly-Si TFT is sufficient to drive pixels of OLEDs, as well as LCDs (Liquid-Crystal Displays), on plastic. However, the obtained mobility value is smaller than the value expected in the SEM image of Figure 3. In order to be utilized at the high speed of peripheral circuits for Active-Matrix FPDs, a much higher mobility value is required of both n-MOS and p-MOS TFTs. Further optimization is required of processes such as ultra-low temperature hydrogenation and organic cleaning as well as ELC so to use them with plastic substrate.

IV. CONCLUSION

The a-Si film was deposited by r.f. sputtering at room temperature as a precursor material for laser crystallization. The incorporated gas content in the a-Si films by Xe sputtering is only 0.39 %. The poly-Si film by laser irradiation of the Xe sputtered a-Si film had a the maximum grain size of 1 µm. After TFT fabrication, the measured field-effect carrier mobility of the poly-Si TFT on quartz and plastic substrate is 70 cm$^2$/V·s and 15 cm$^2$/V·s, respectively.

REFERENCES